



10

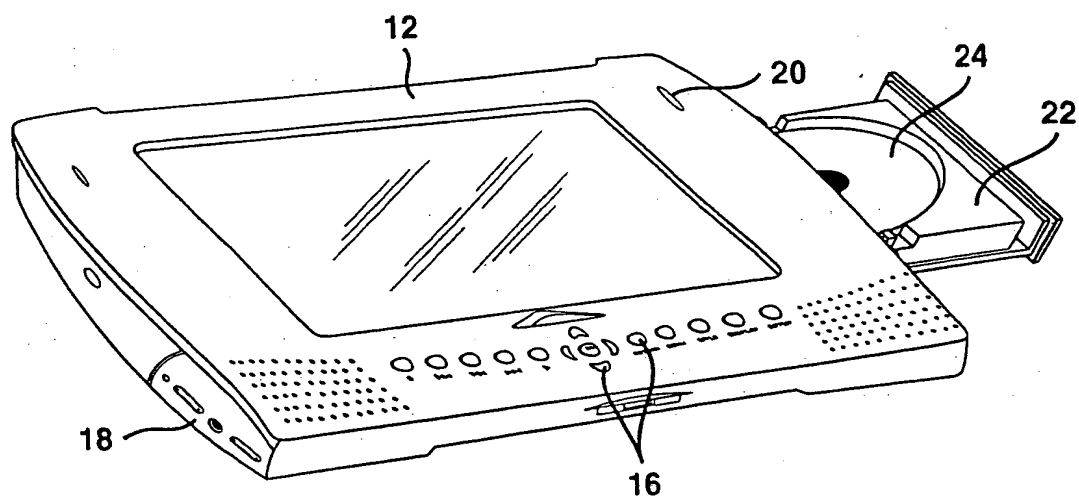


Fig. 1A

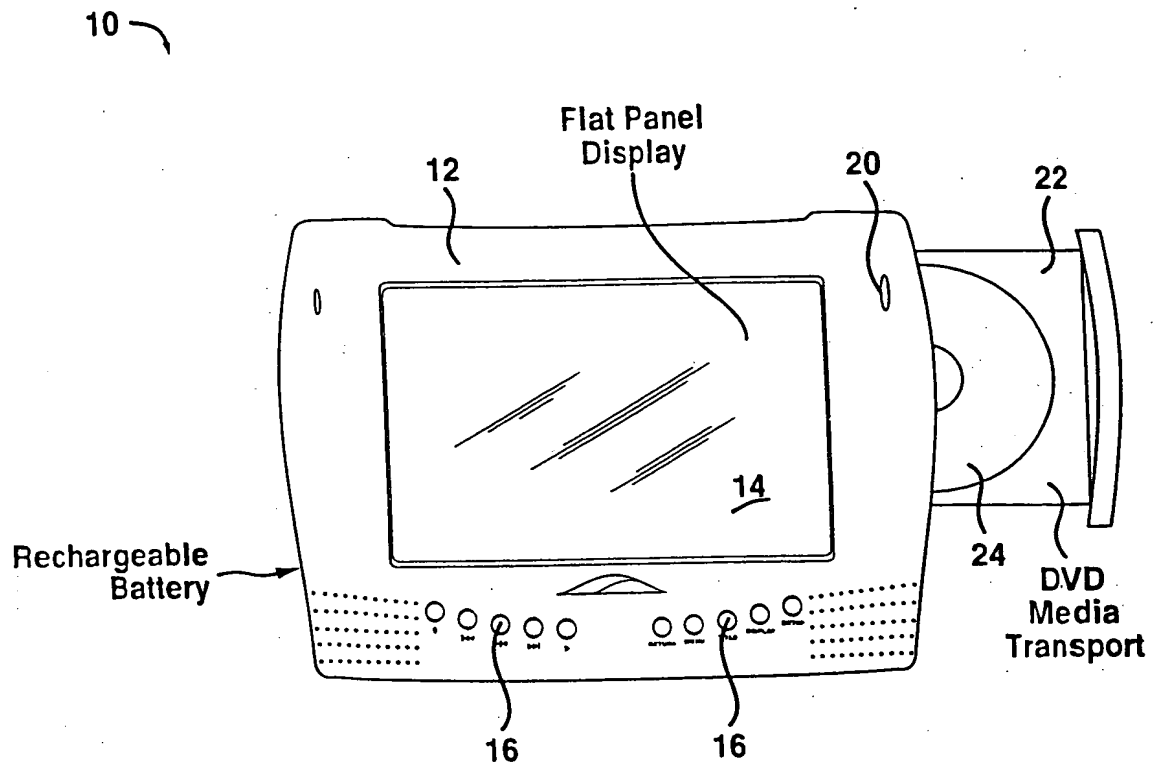


Fig. 1B

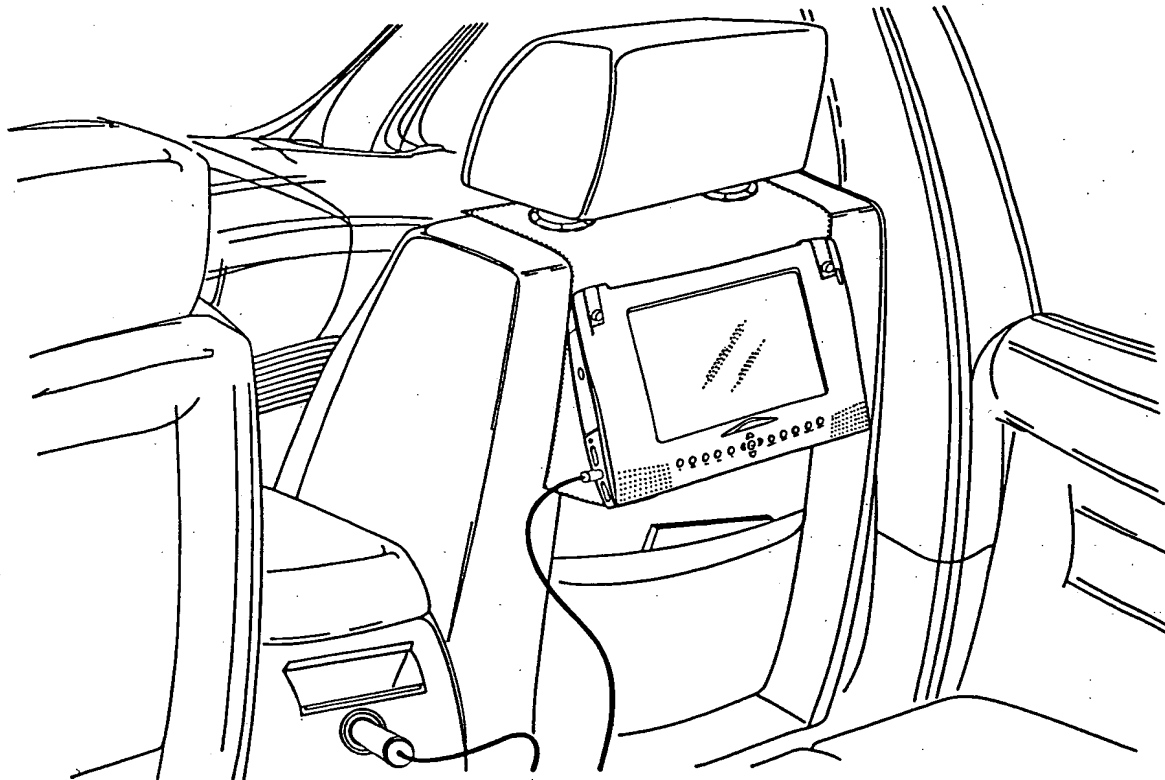


Fig. 2A

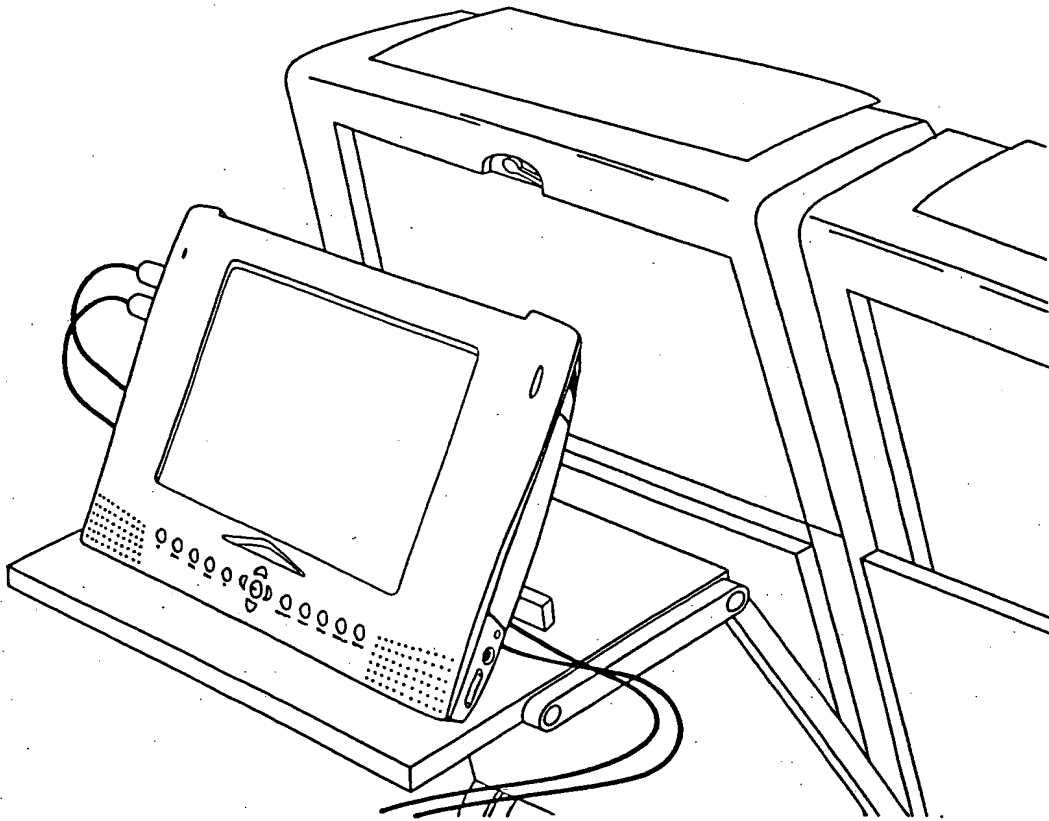


Fig. 2B



Fig. 2C

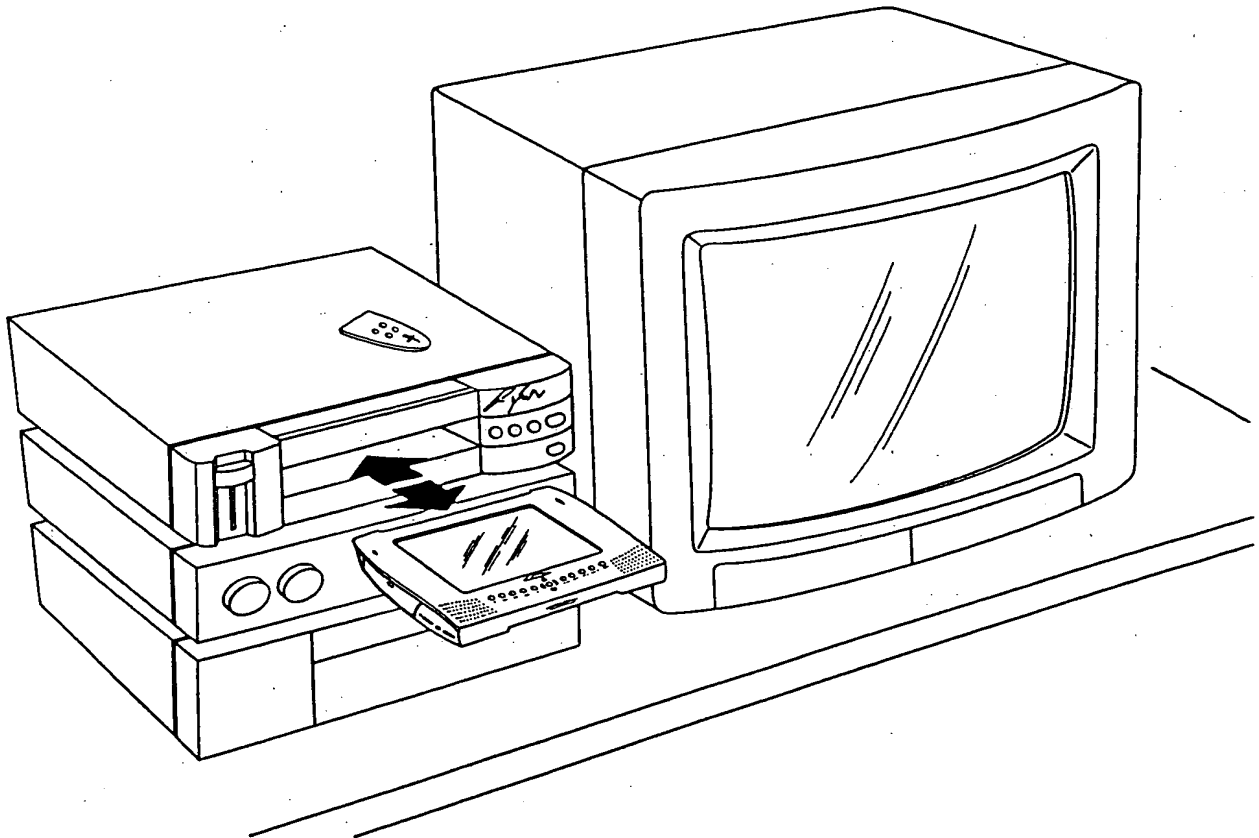


Fig. 2D

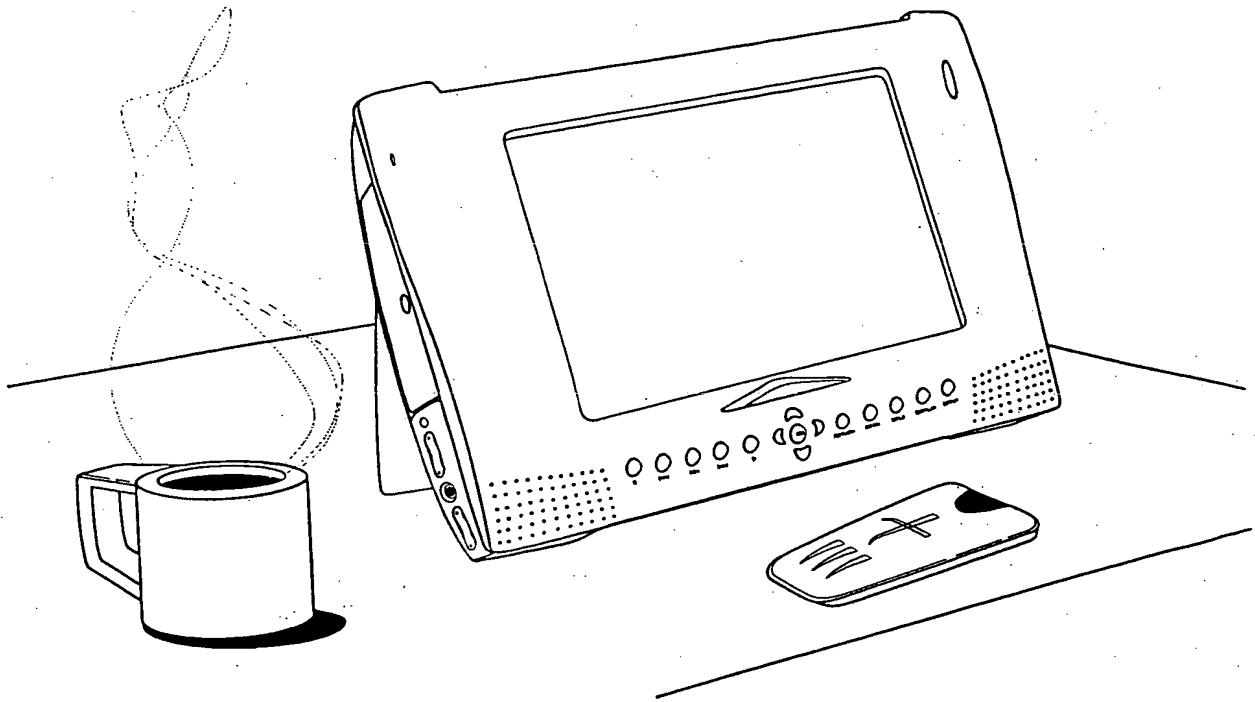


Fig. 2E

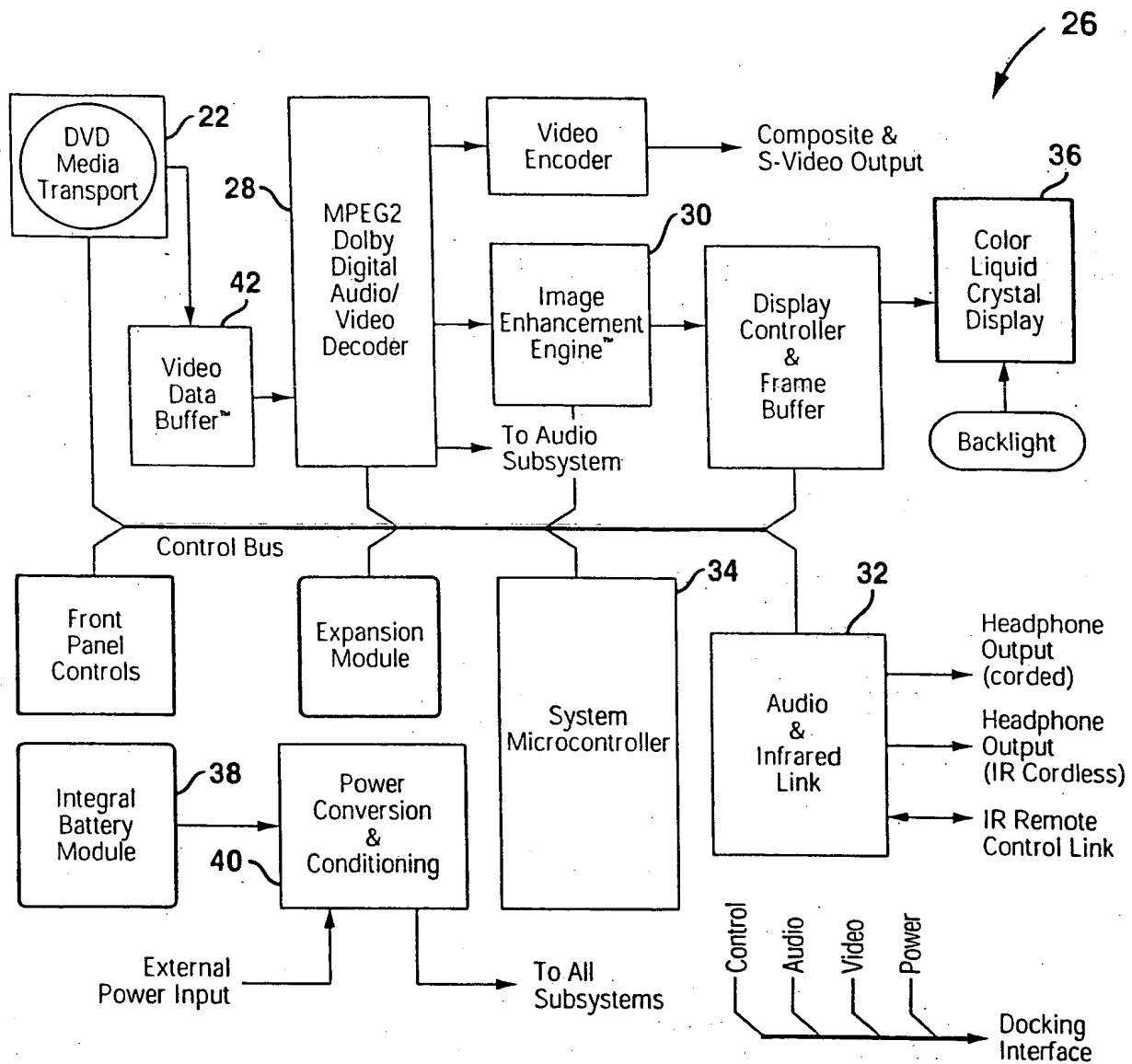


Fig. 3

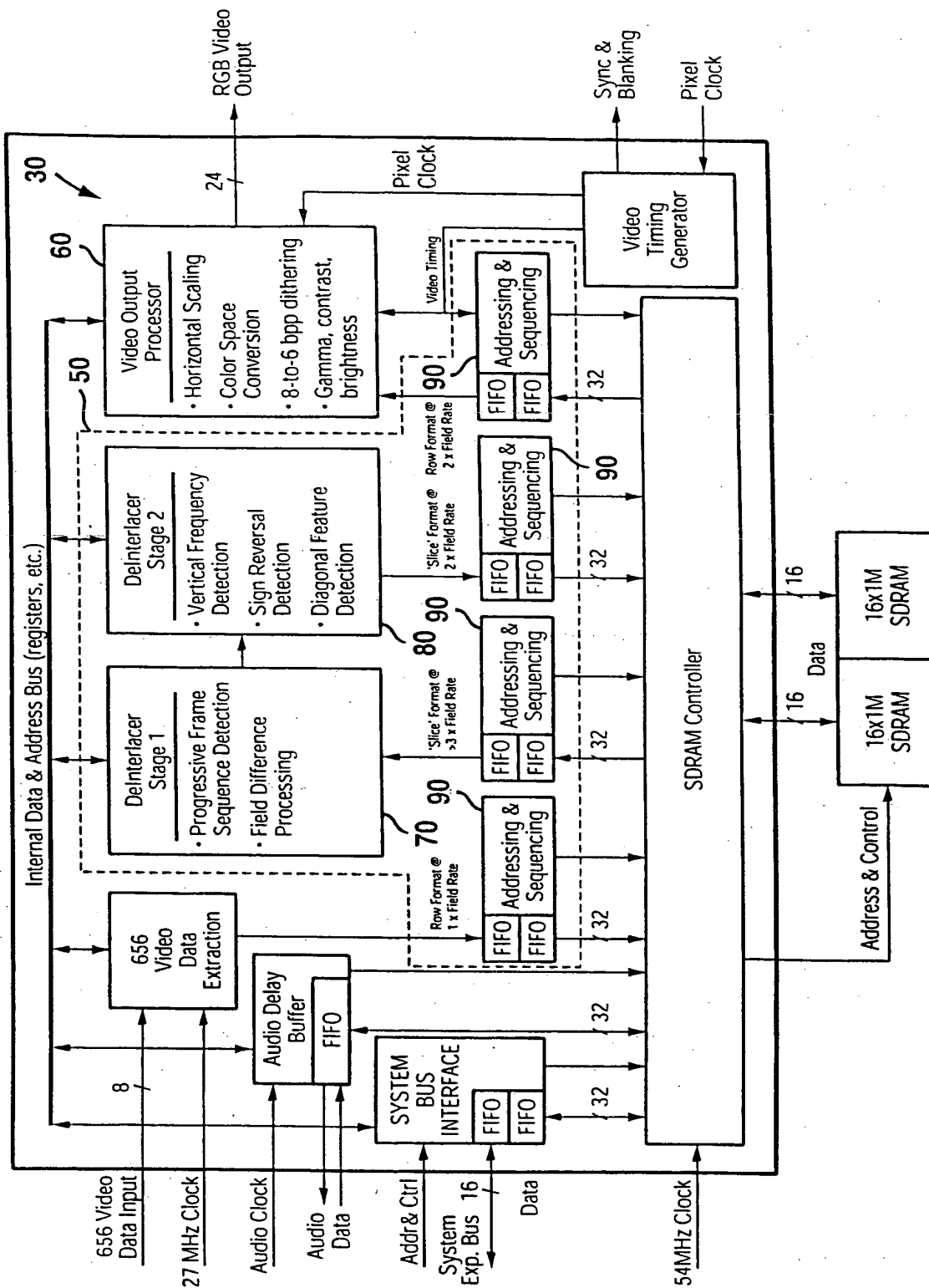


Fig. 4

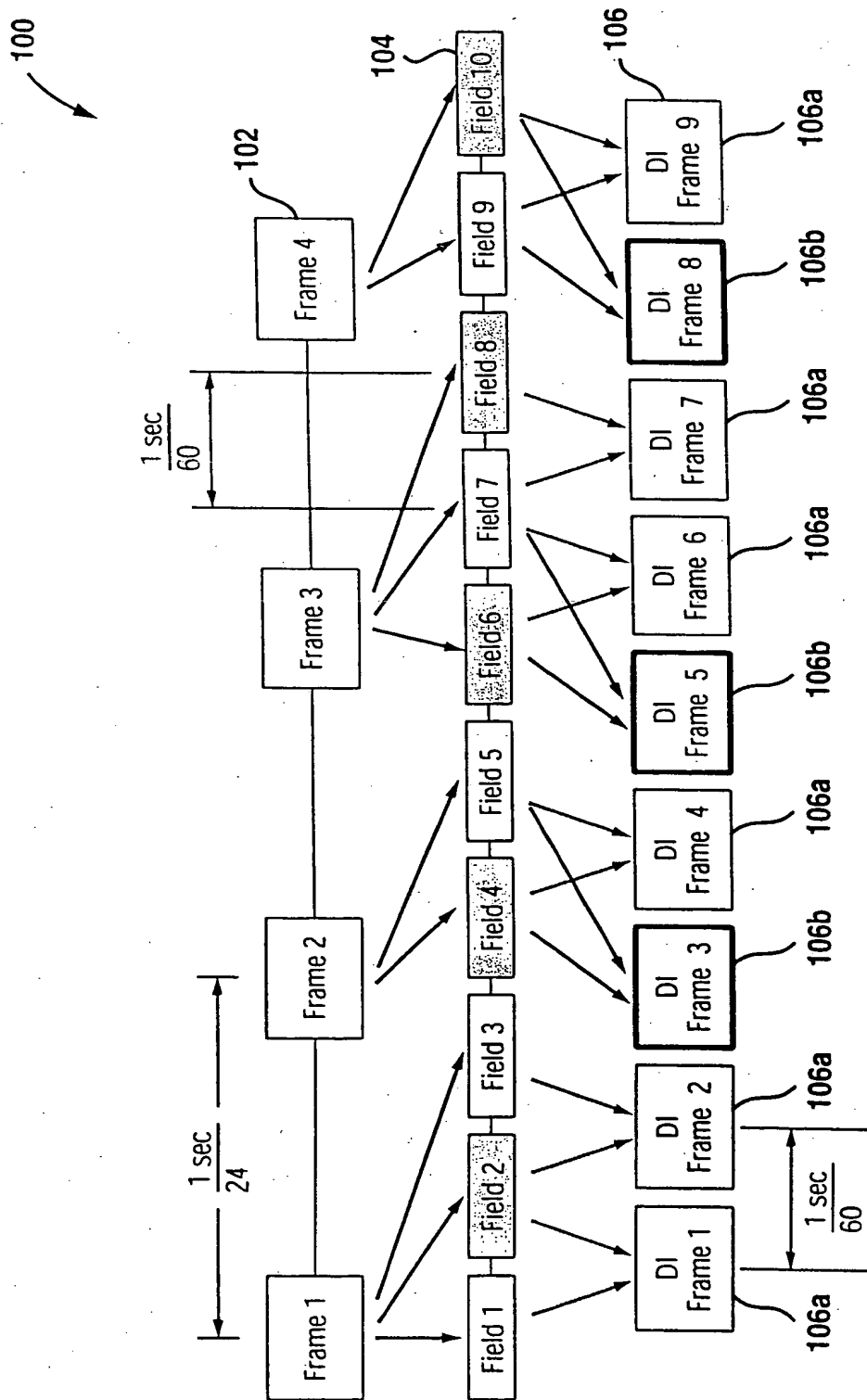


Fig. 5

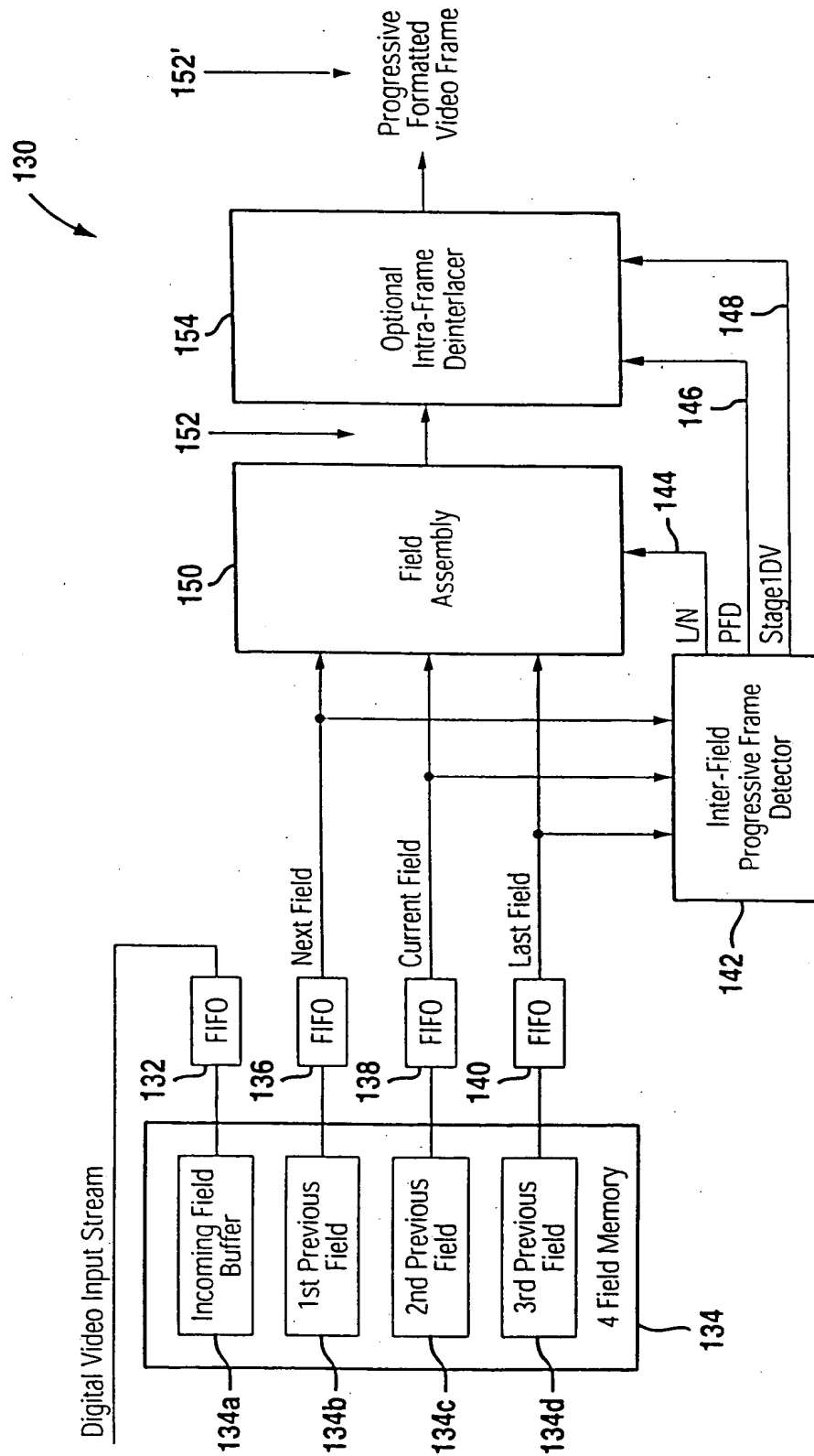


Fig. 6

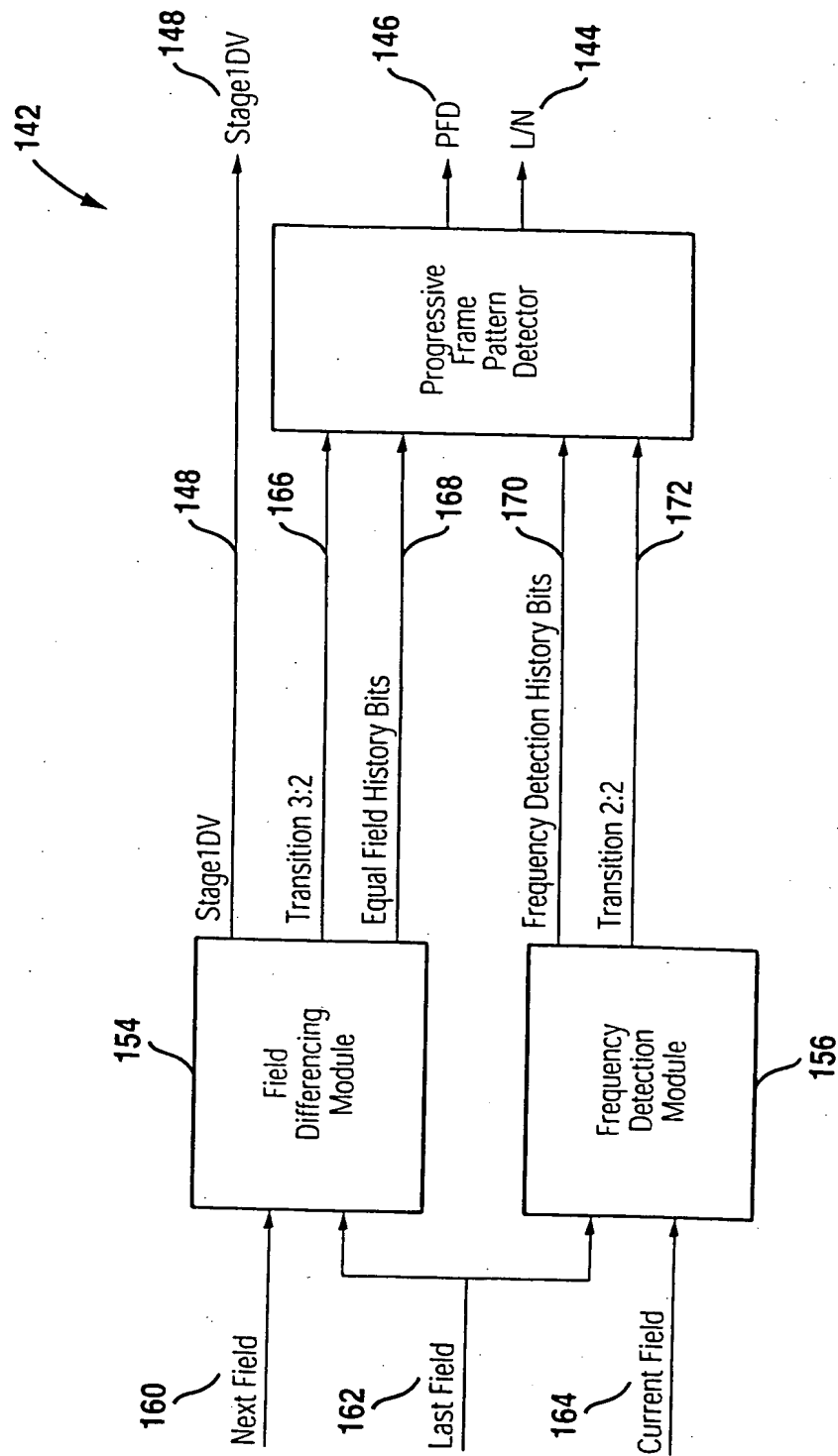


Fig. 7

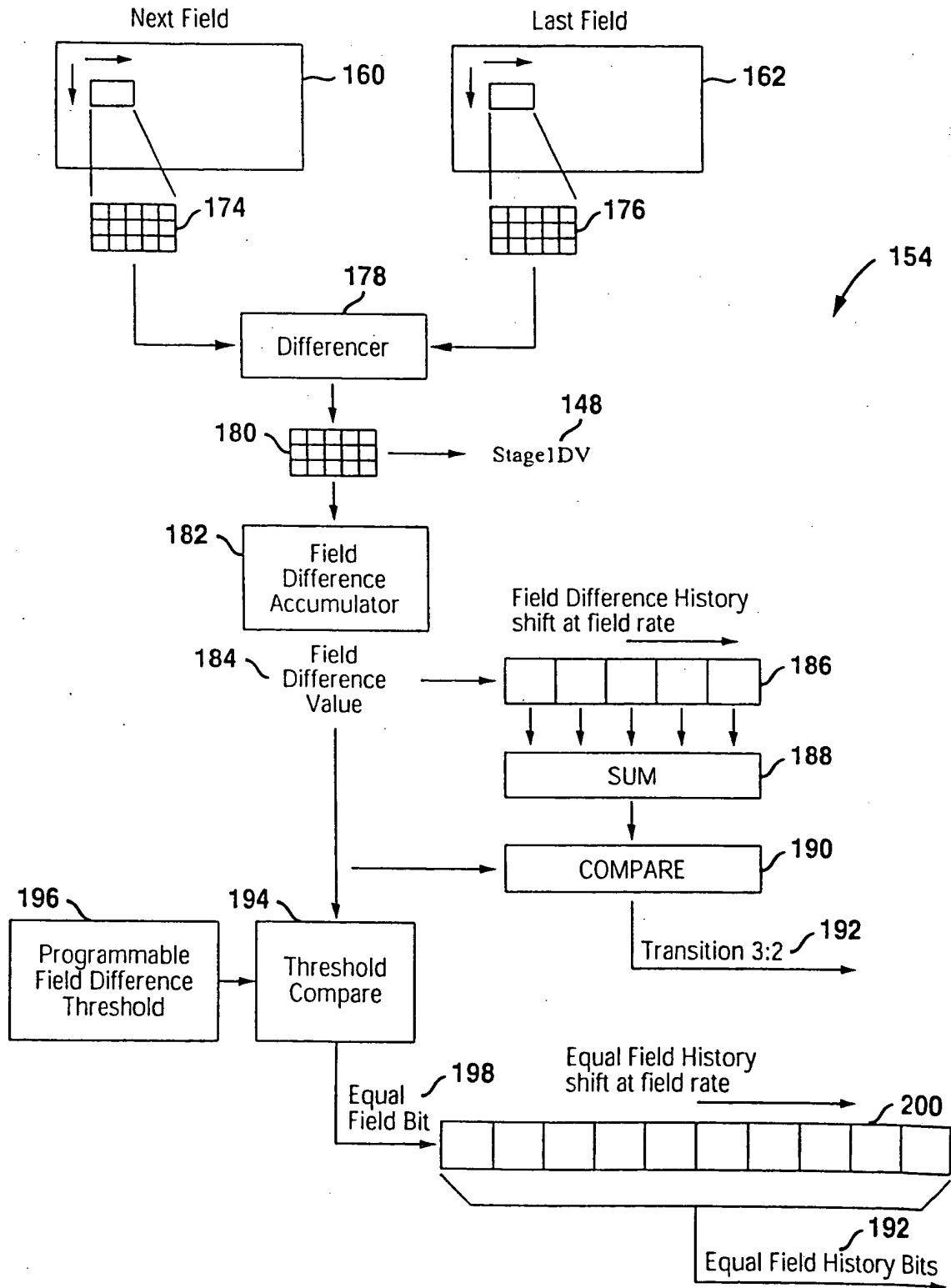


Fig. 8

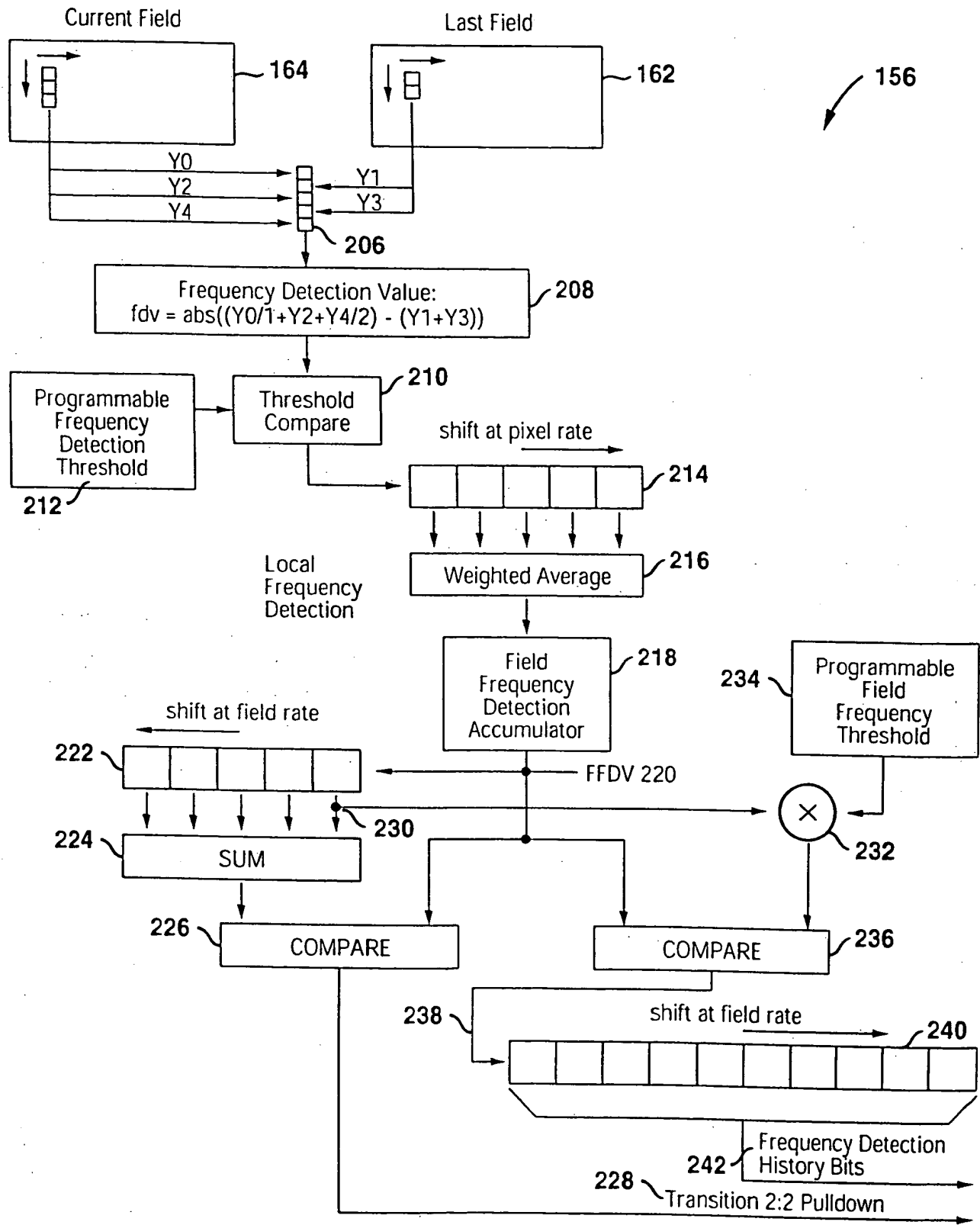


Fig. 9

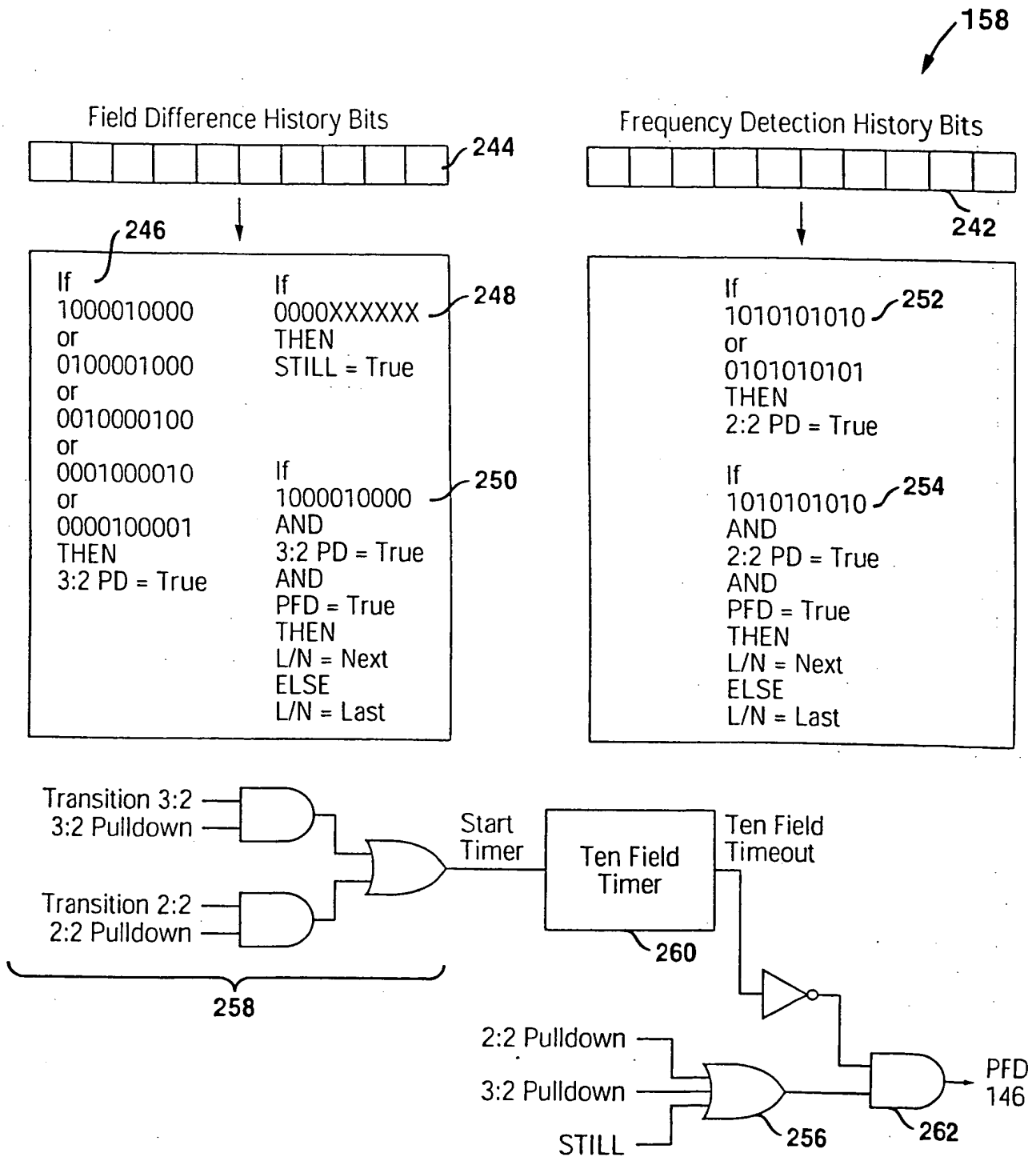


Fig. 10

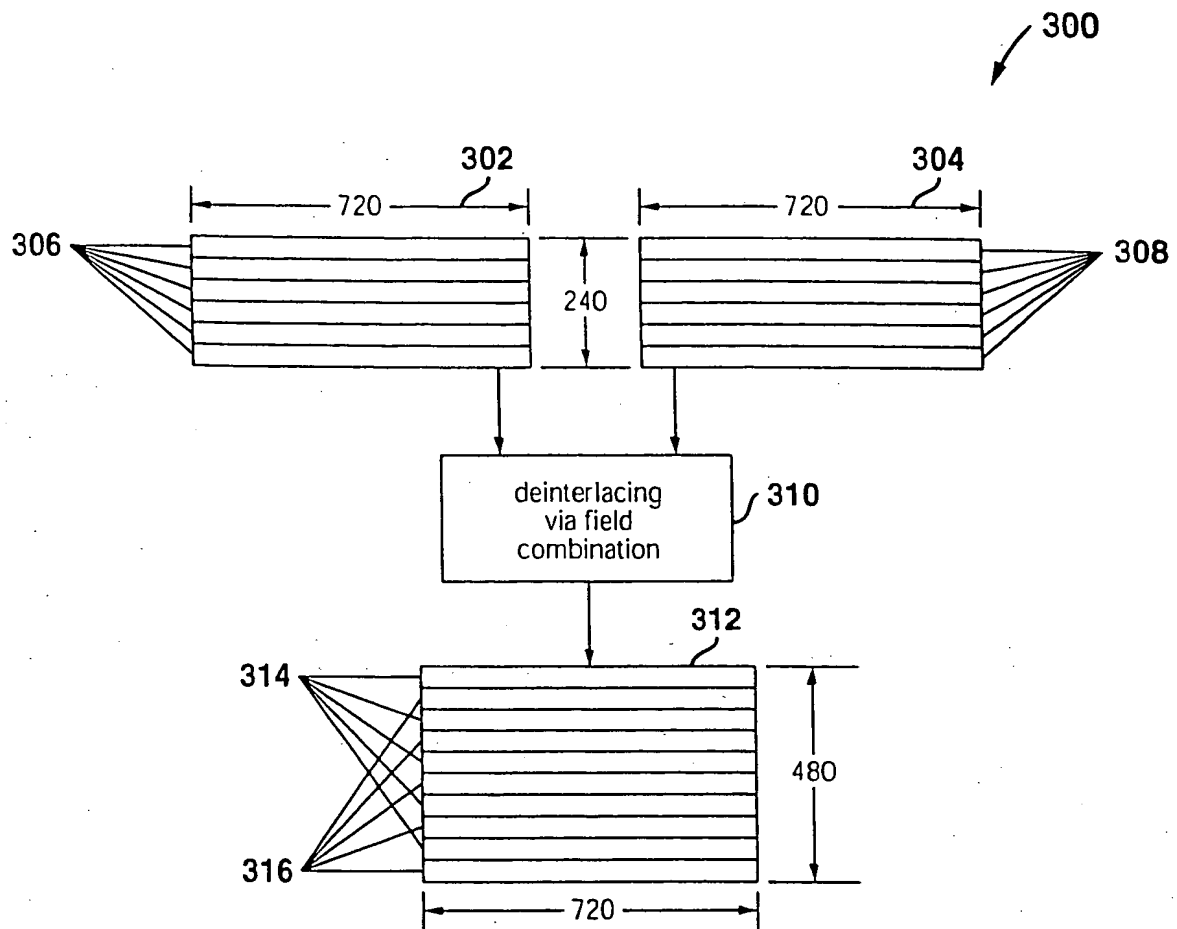


Fig. 11

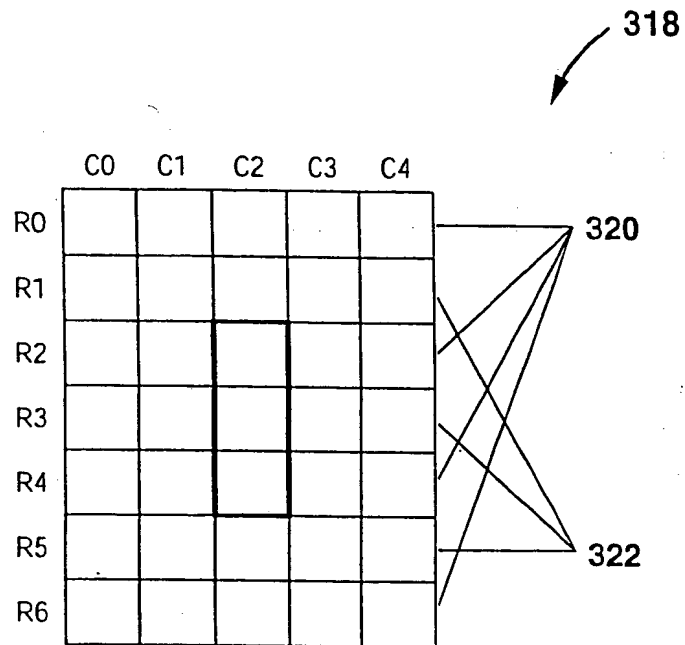


Fig. 12

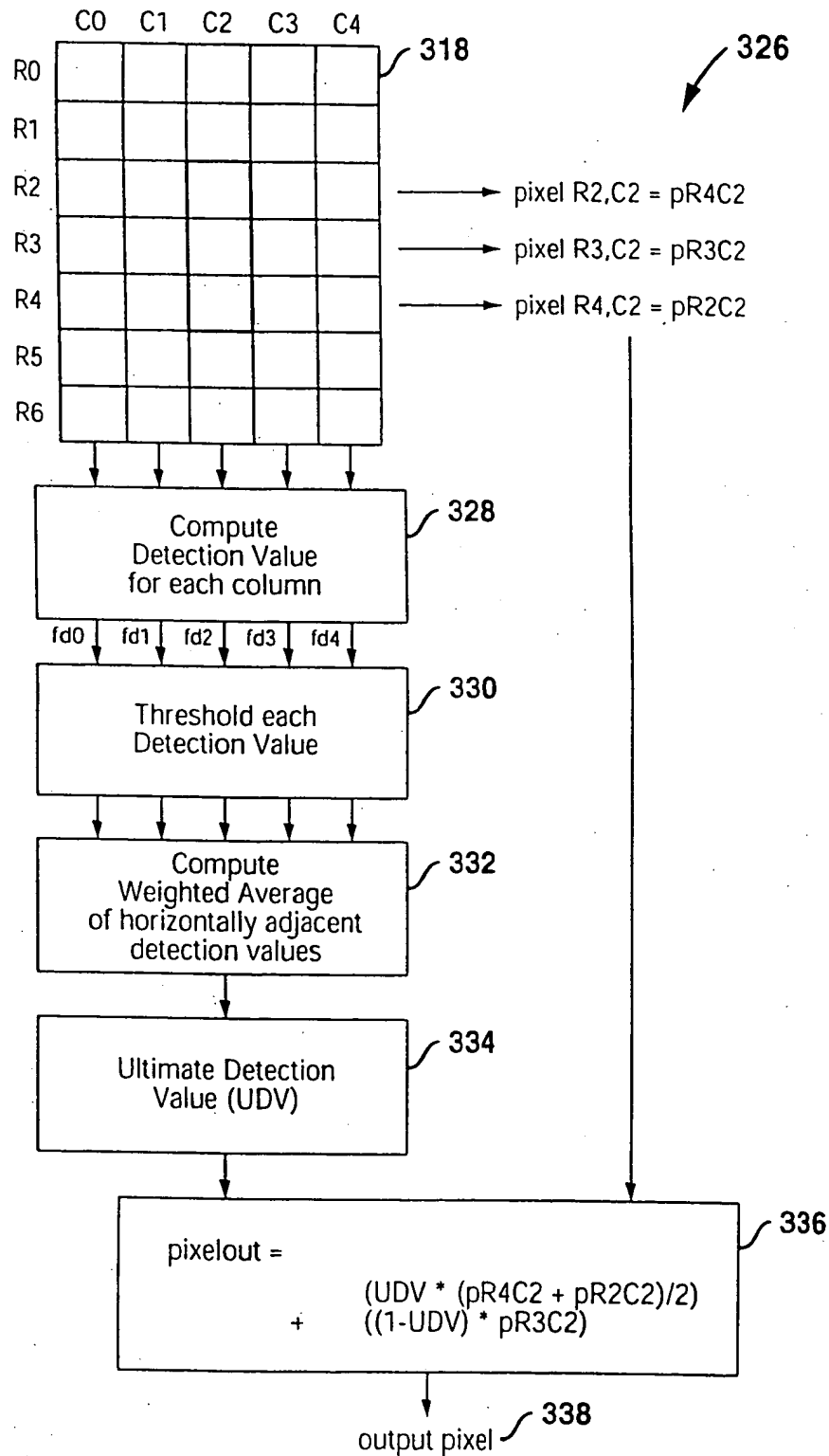


Fig. 13

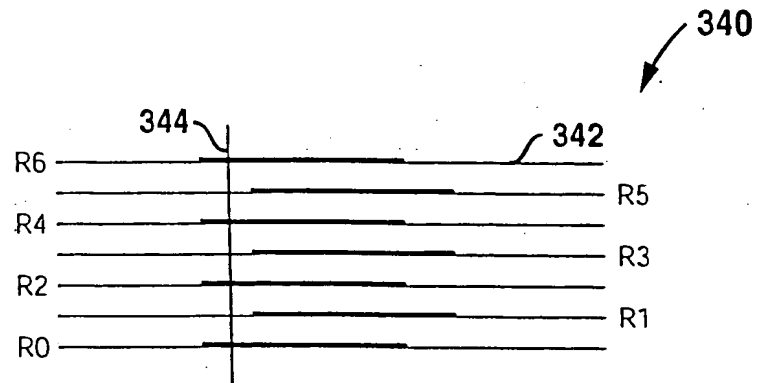


Fig. 14A

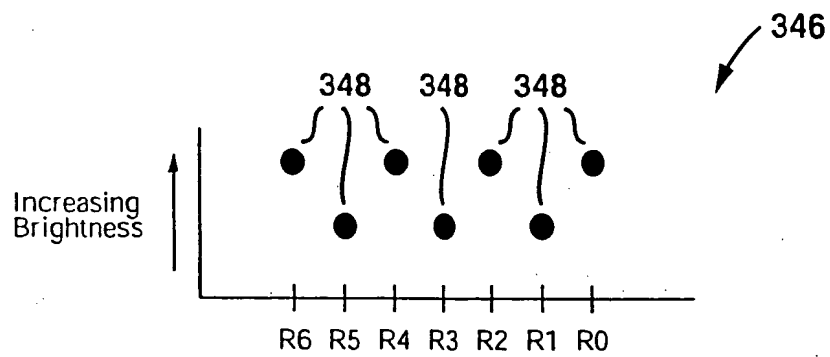


Fig. 14B

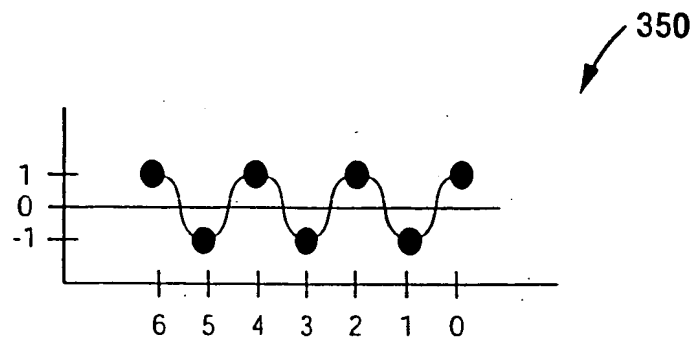


Fig. 14C

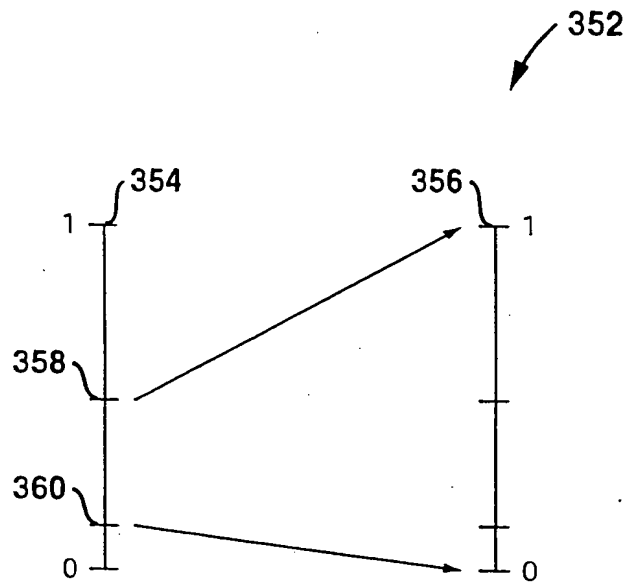


Fig. 15

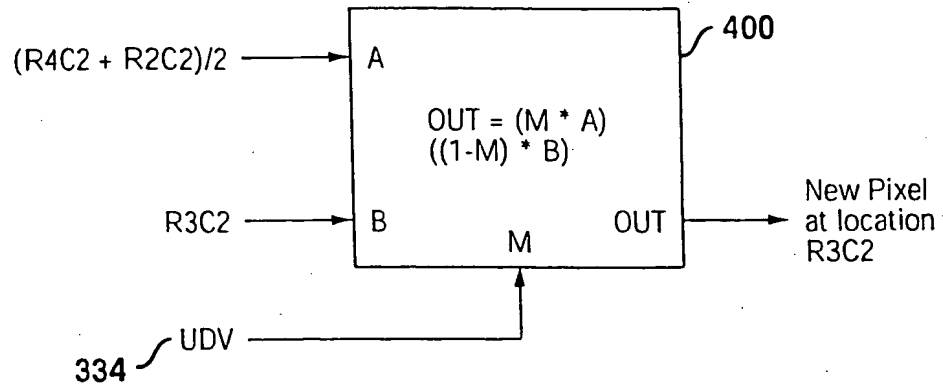


Fig. 16

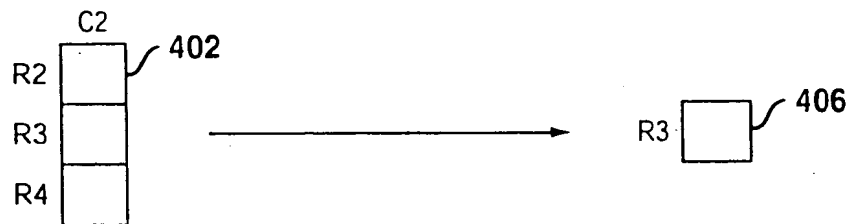


Fig. 17

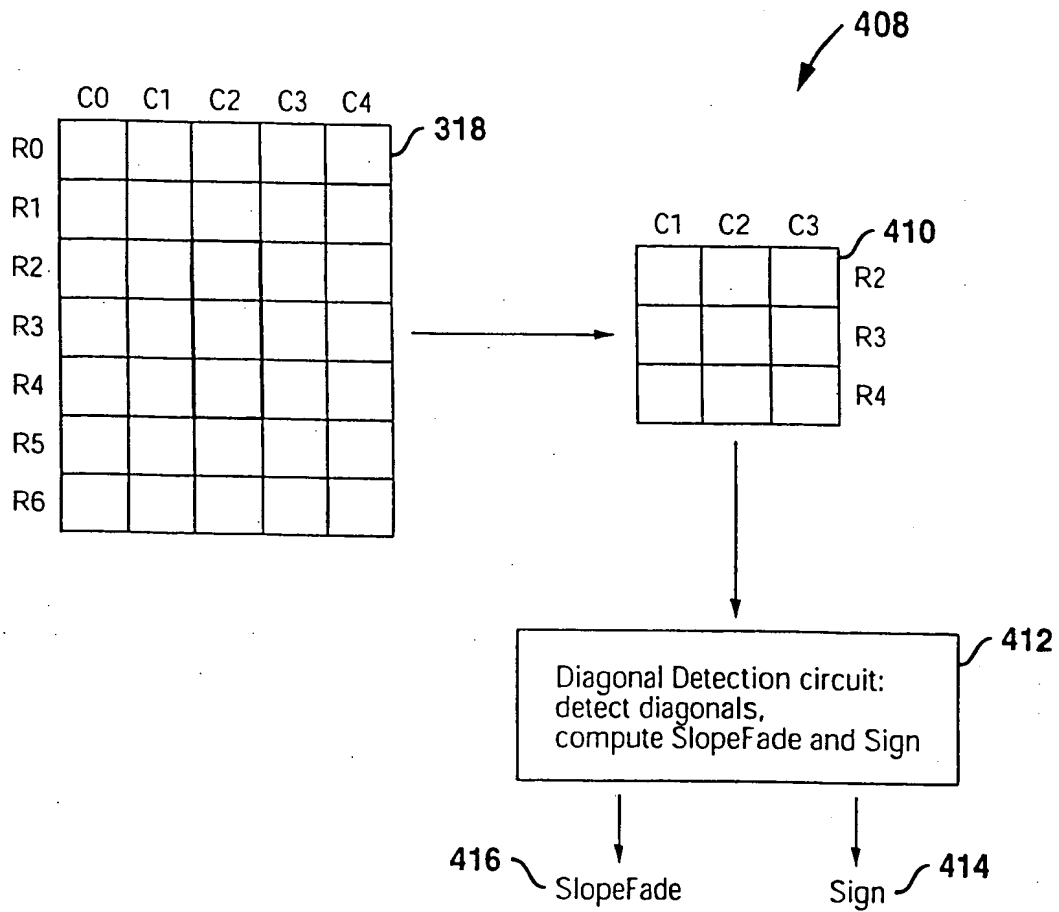


Fig. 18

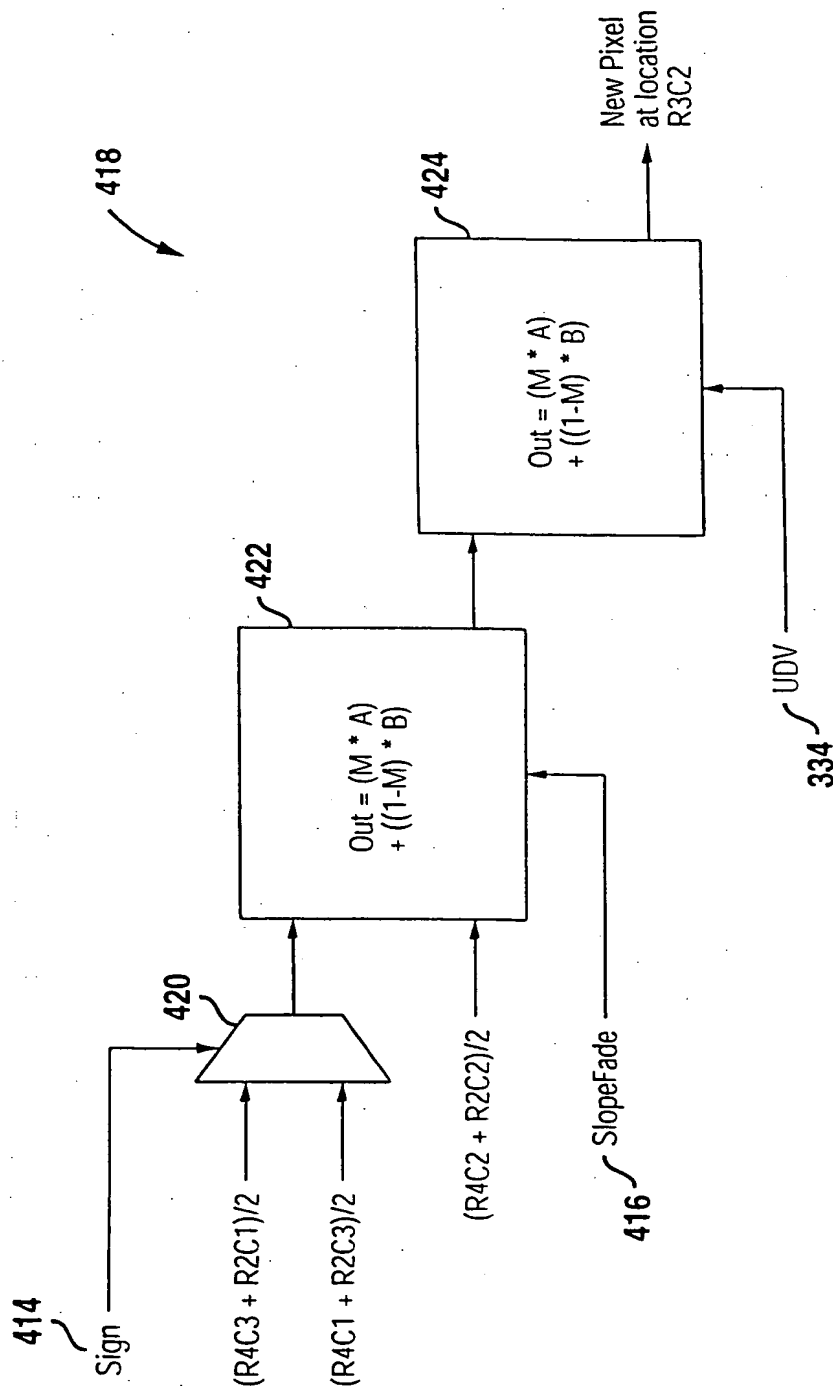


Fig. 19

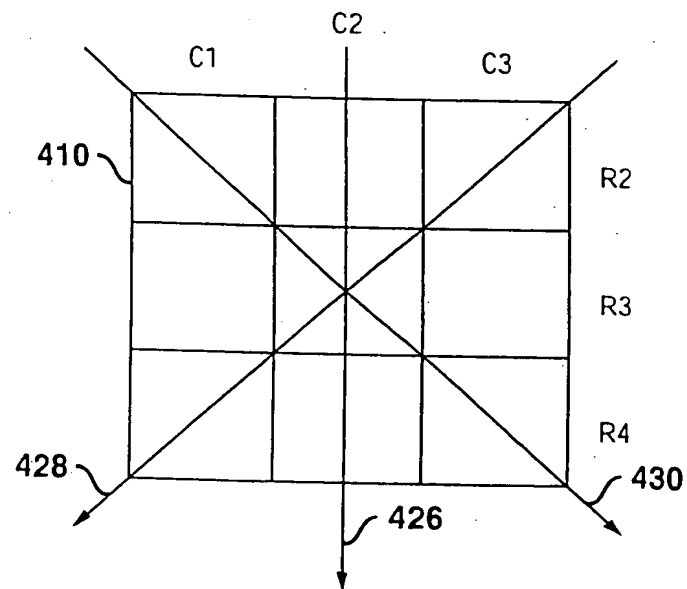
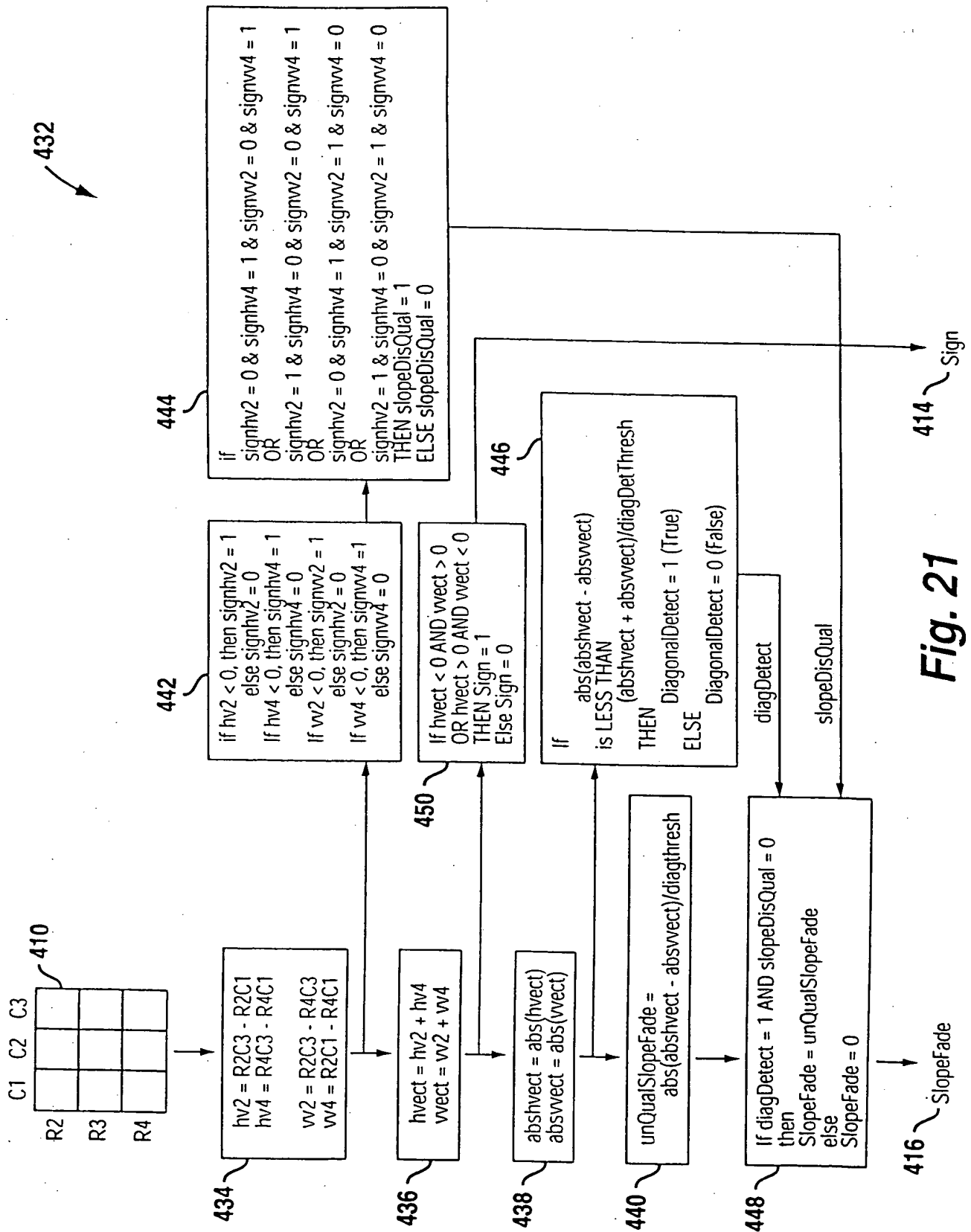


Fig. 20



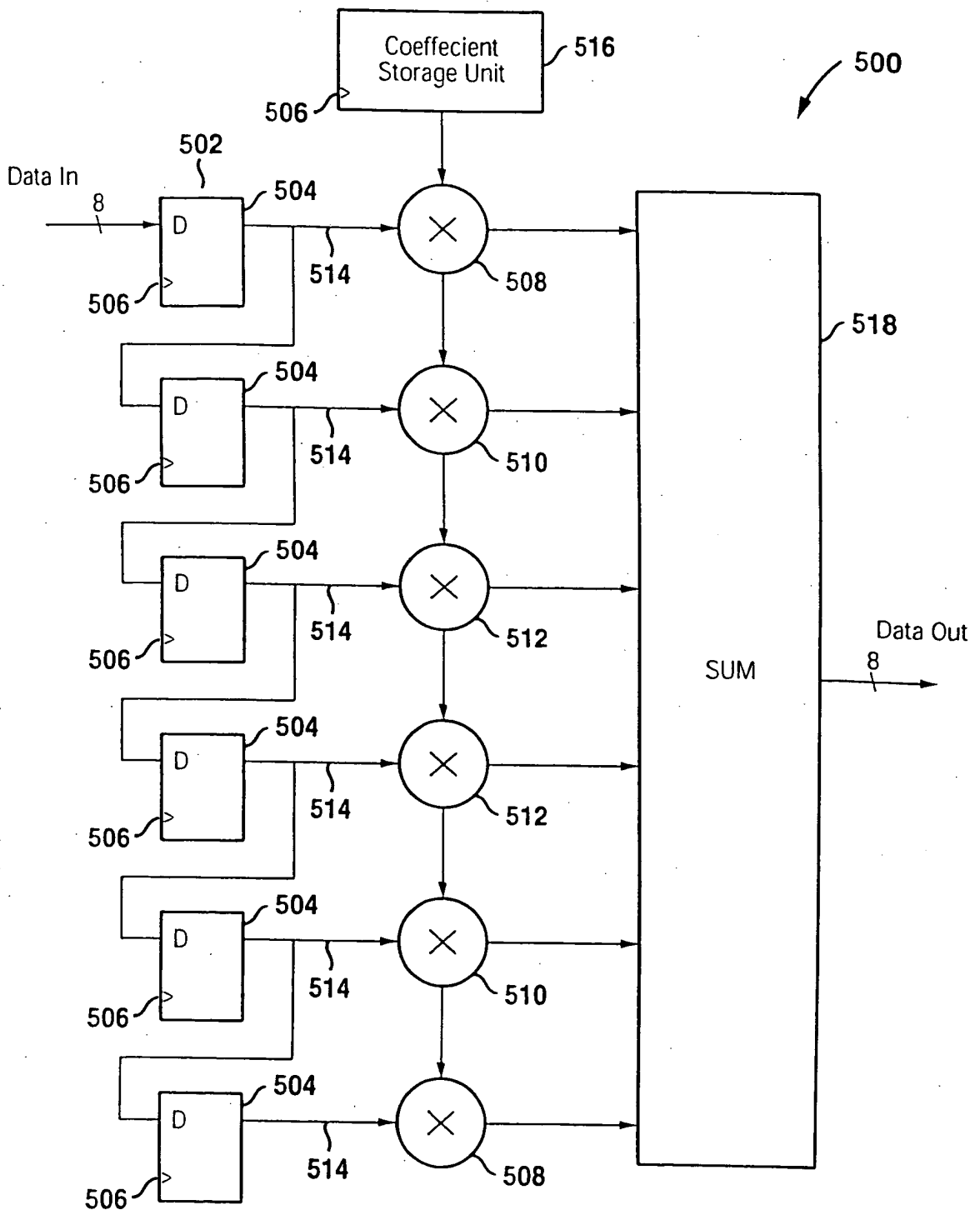


Fig. 22

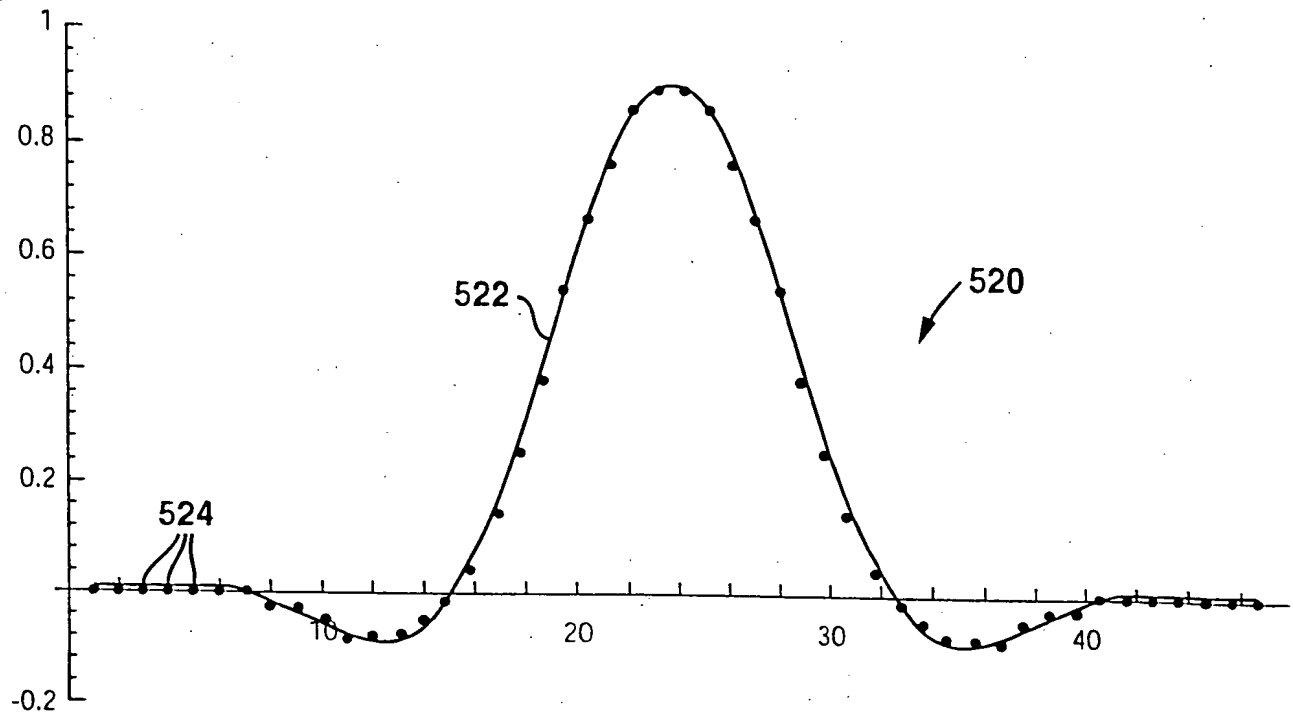
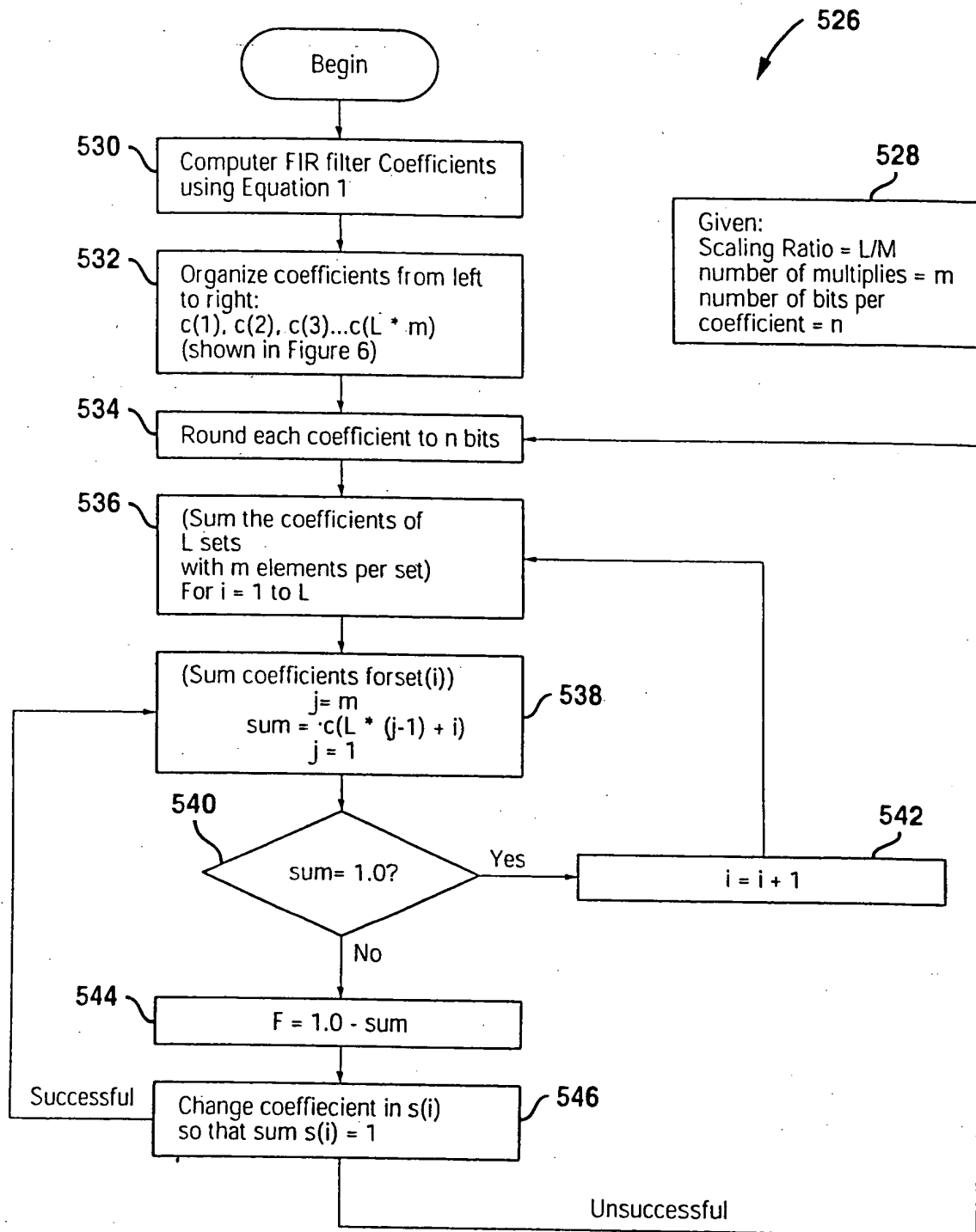


Fig. 23

set(1)	c(1), c(9), c(17), c(25), c(33), c(41)
set(2)	c(2), c(10), c(18), c(26), c(34), c(42)
set(3)	c(3), c(11), c(19), c(27), c(35), c(43)
set(4)	c(4), c(12), c(20), c(28), c(36), c(44)
set(5)	c(5), c(13), c(21), c(29), c(37), c(45)
set(6)	c(6), c(14), c(22), c(30), c(38), c(46)
set(7)	c(7), c(15), c(23), c(31), c(39), c(47)
set(8)	c(8), c(16), c(24), c(32), c(40), c(48)

Fig. 24

**Fig. 25**

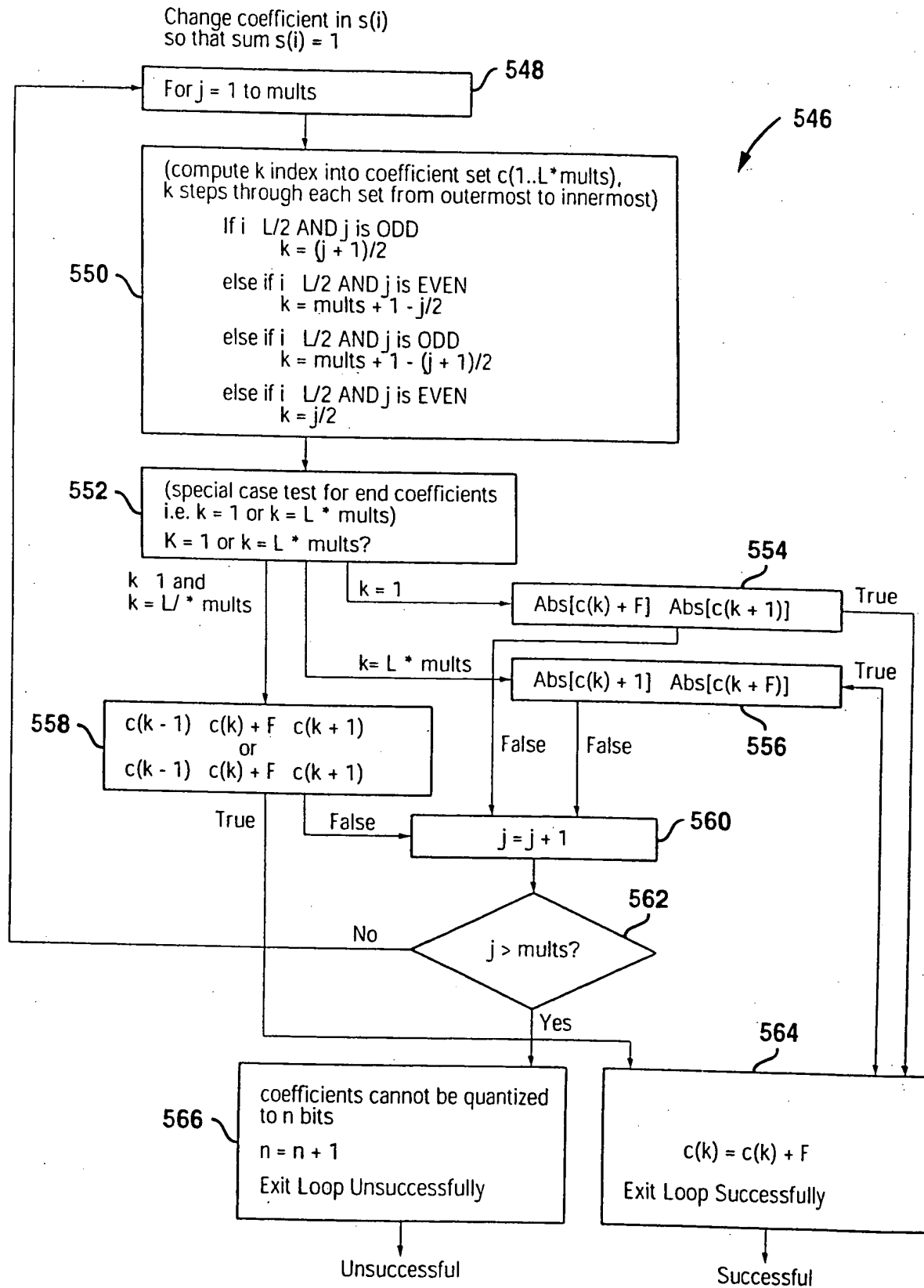


Fig. 26

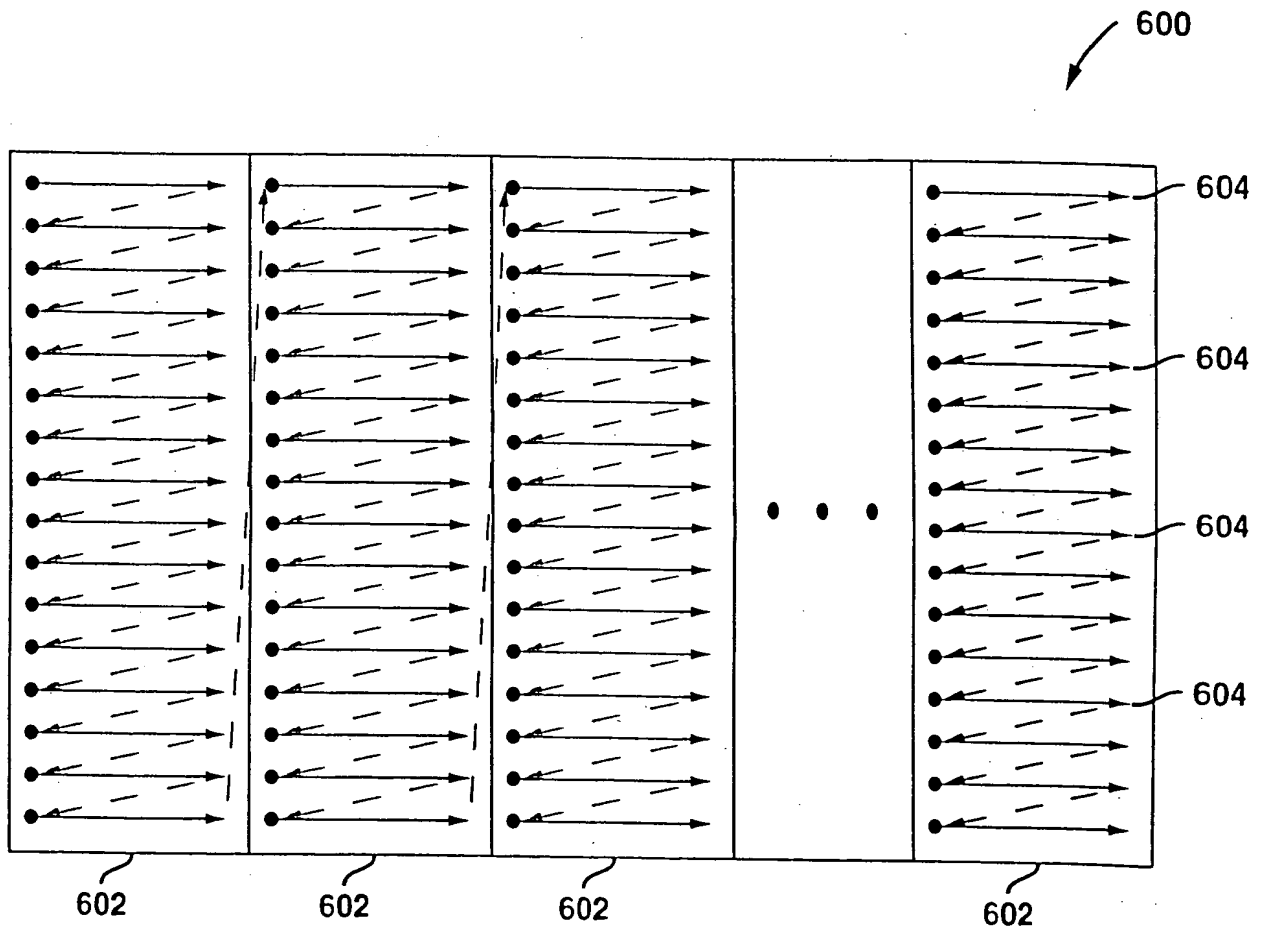


Fig. 27

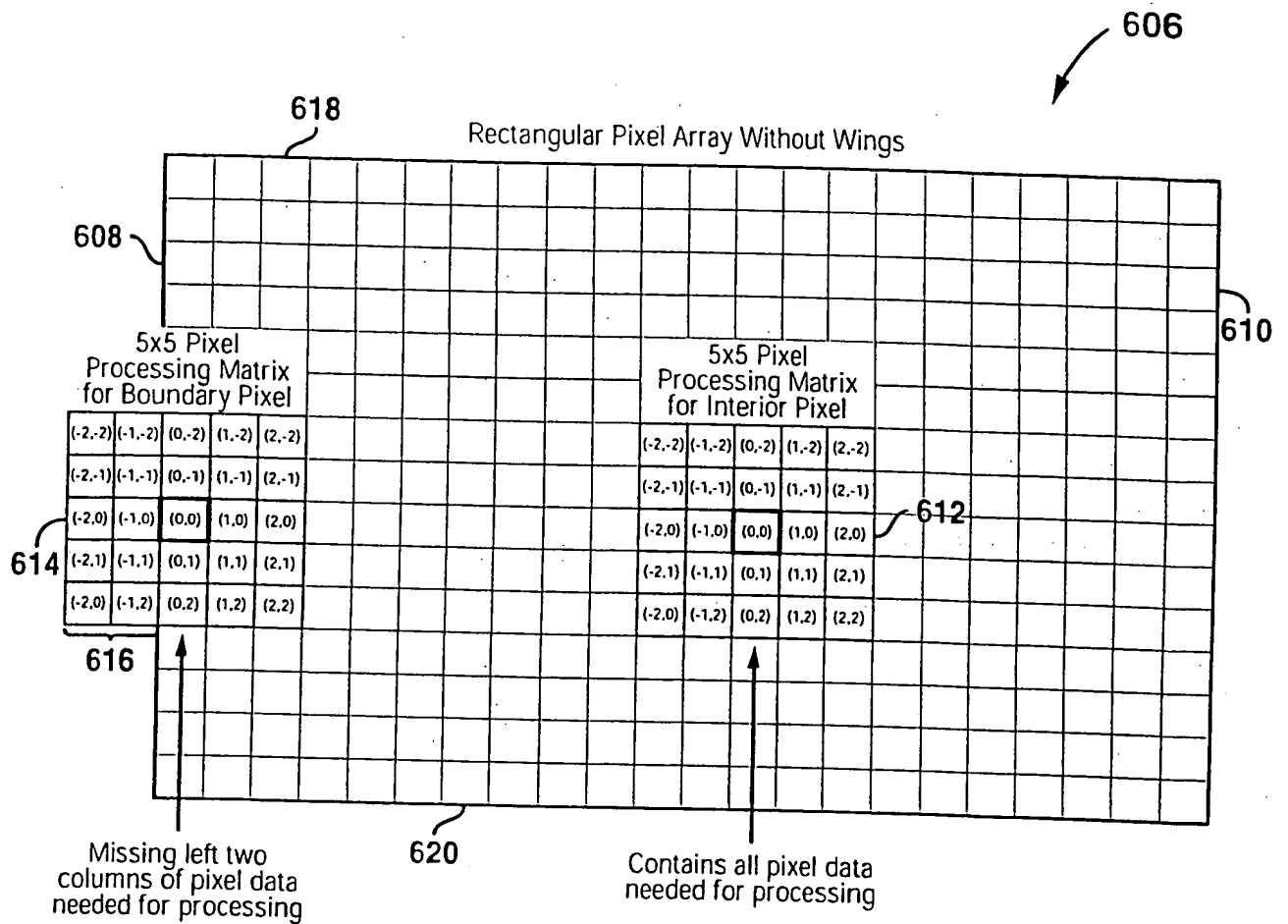


Fig. 28

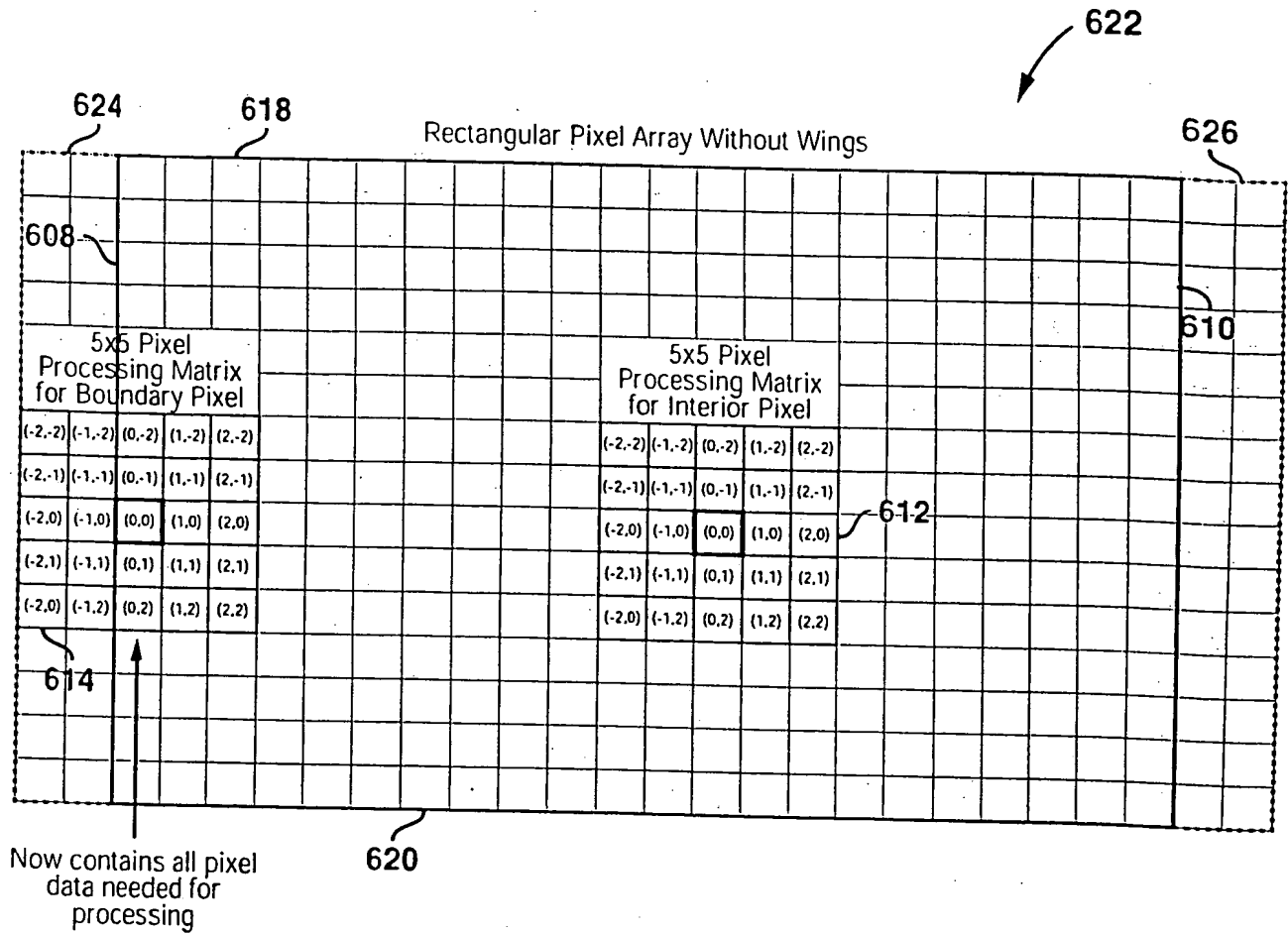


Fig. 29

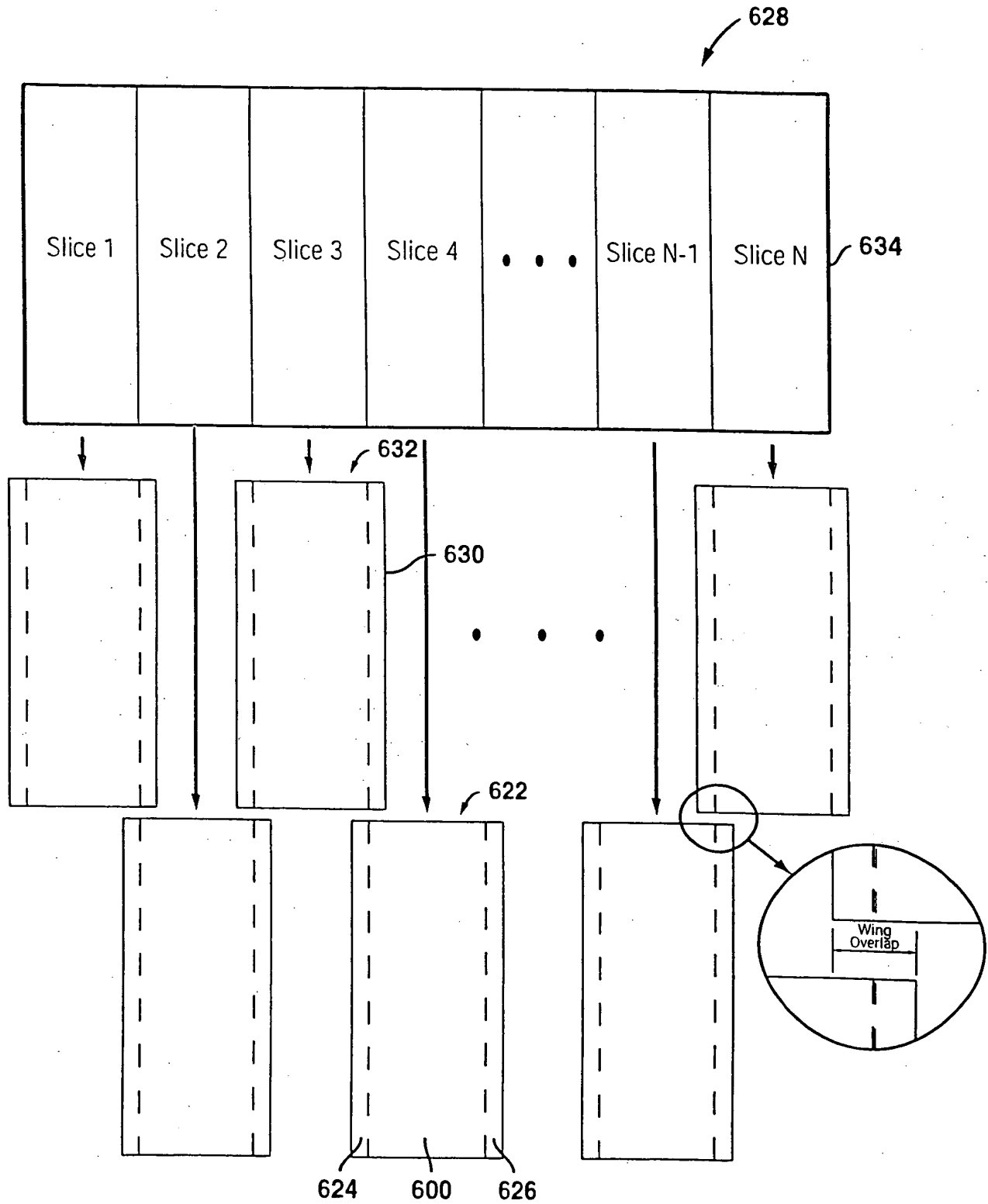


Fig. 30

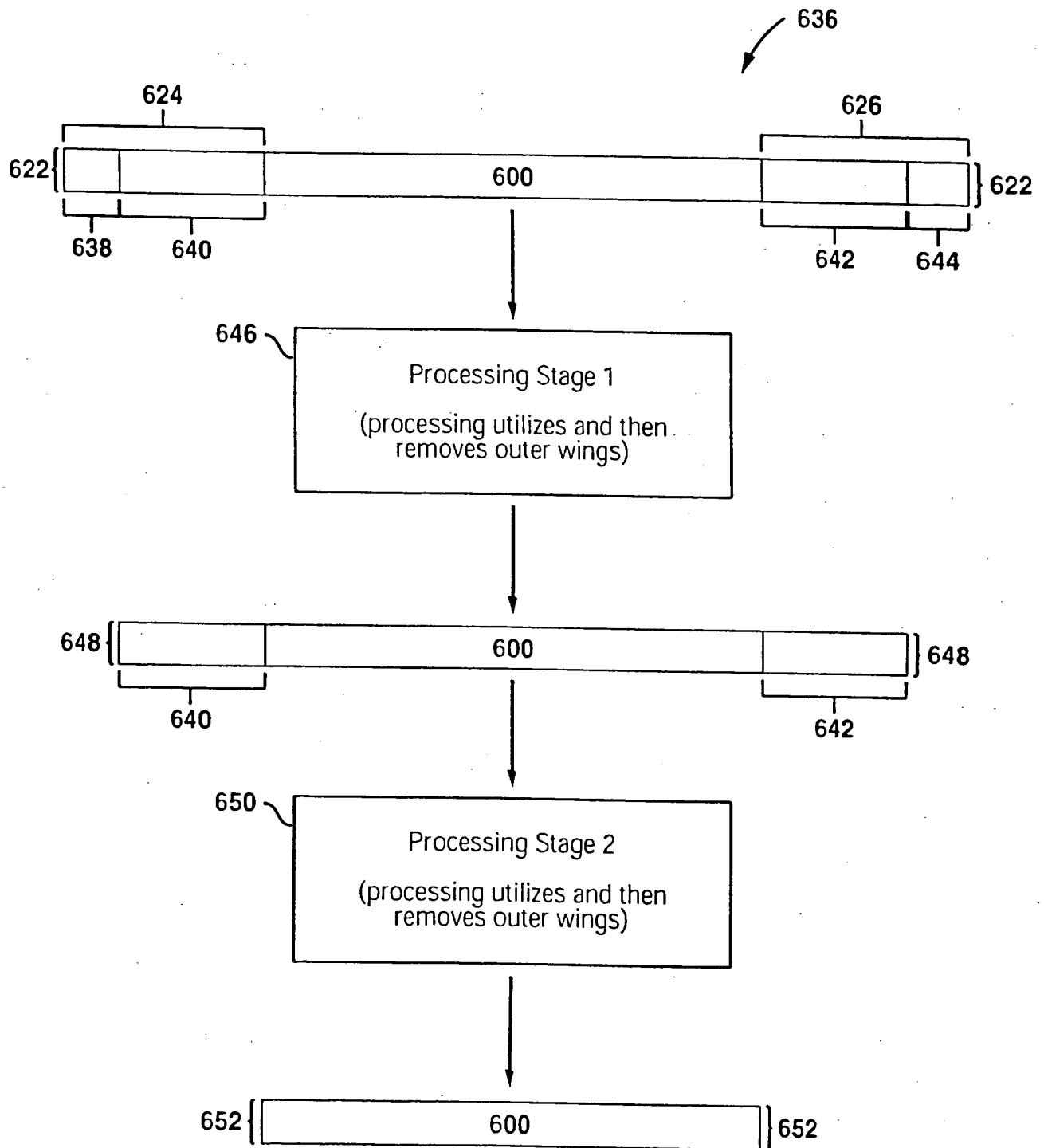


Fig. 31

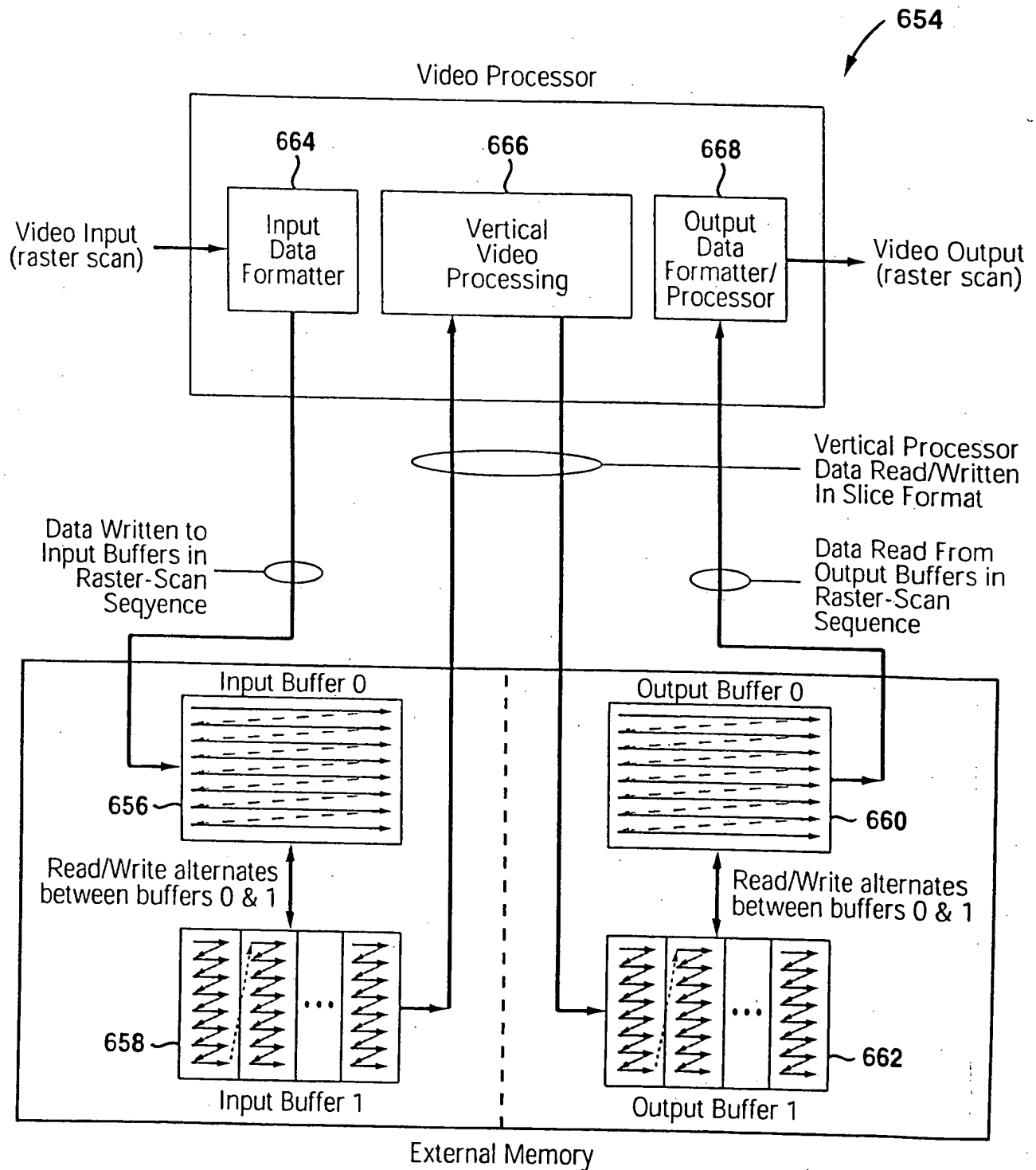


Fig. 32

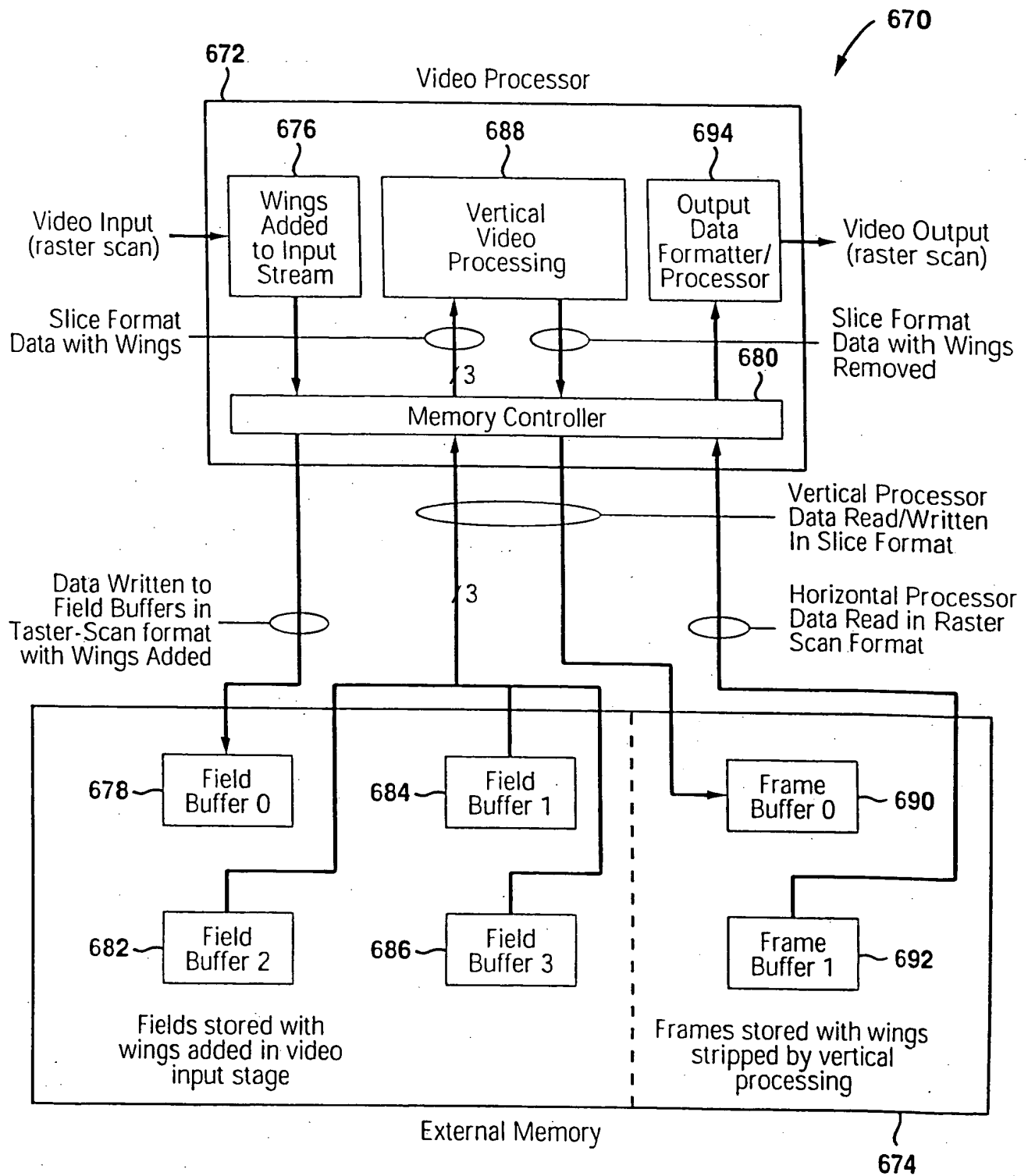


Fig. 33

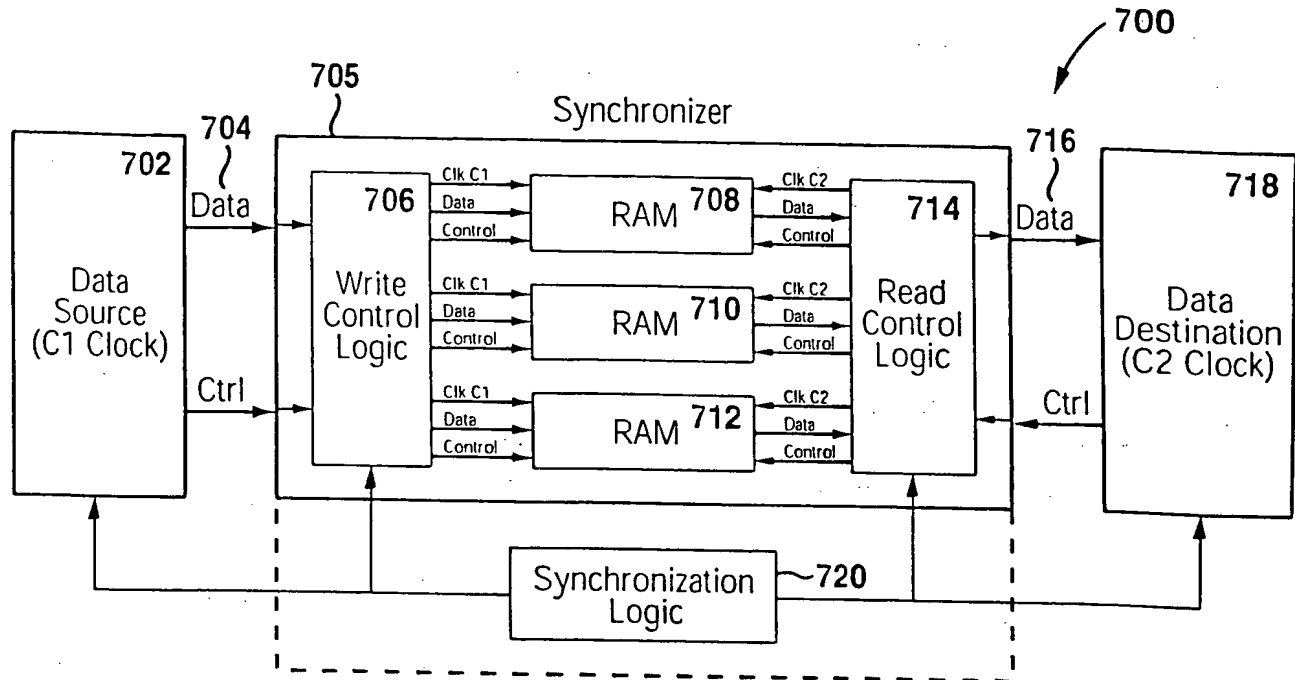


Fig. 34

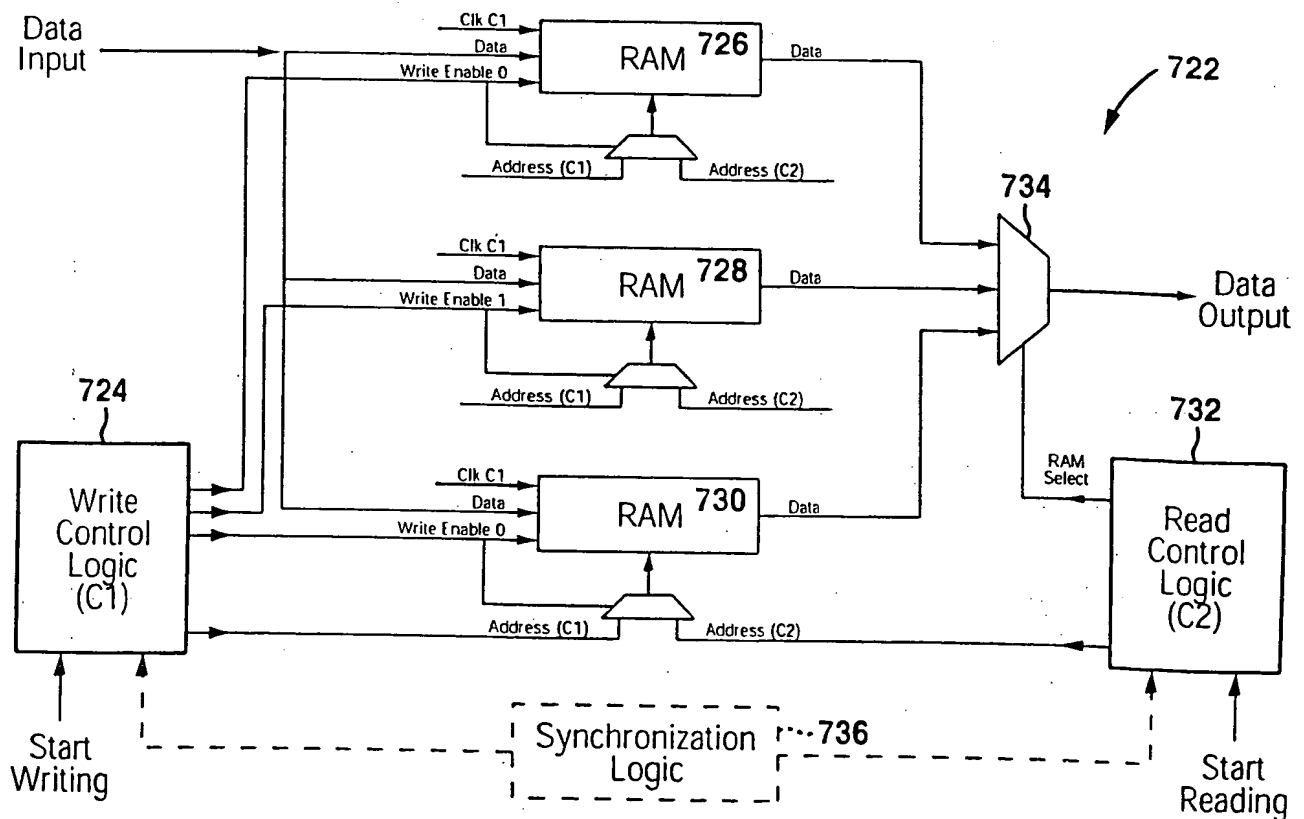
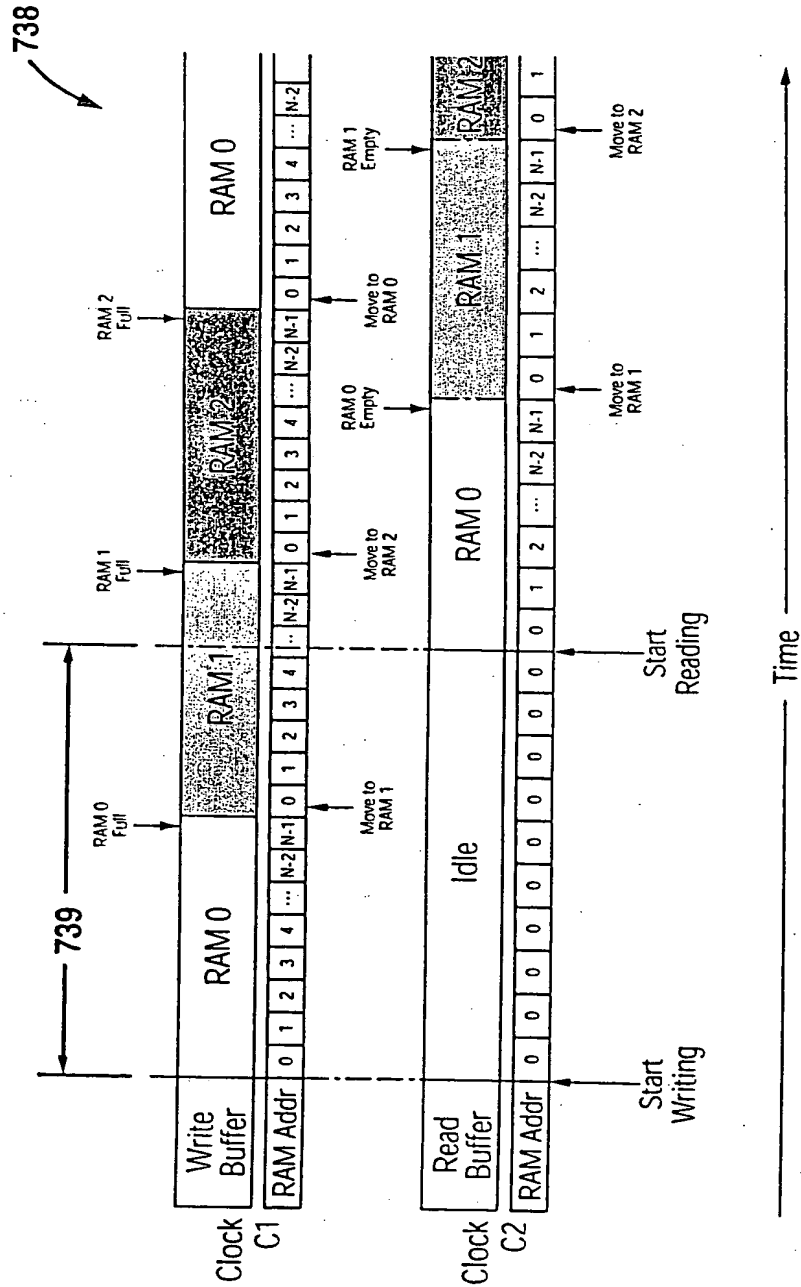
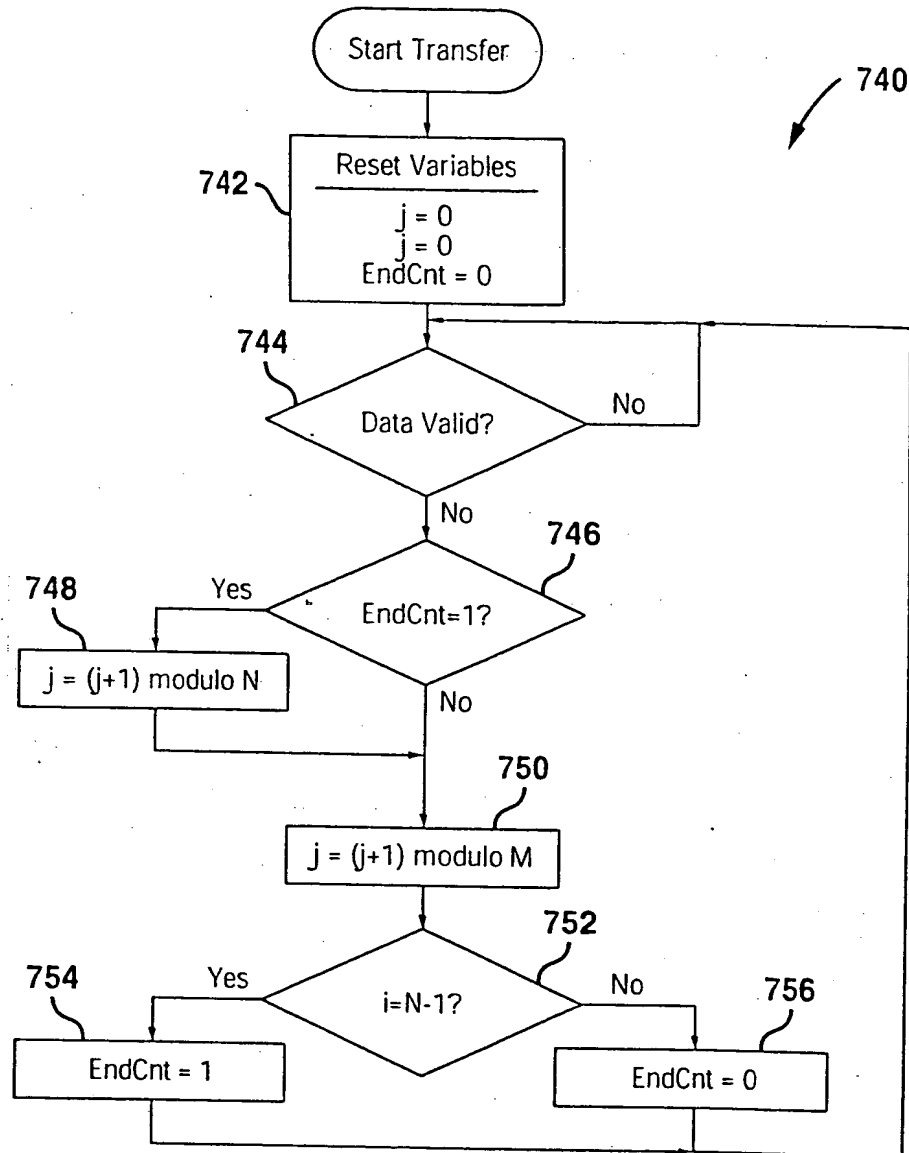


Fig. 35



NOTE: Each RAM has n addressable locations.

Fig. 36



- NOTES: 1. "i" is the RAM Address.
 2. "j" denotes the selected RAM module the address MUX control and RAM write enable.
 3. "EndCnt" indicates that the RAM Address points to the last location in a RAM module.
 4. "M" is the number of addressable location in a RAM module.
 5. "N" is the number of RAM modules.

Fig. 37

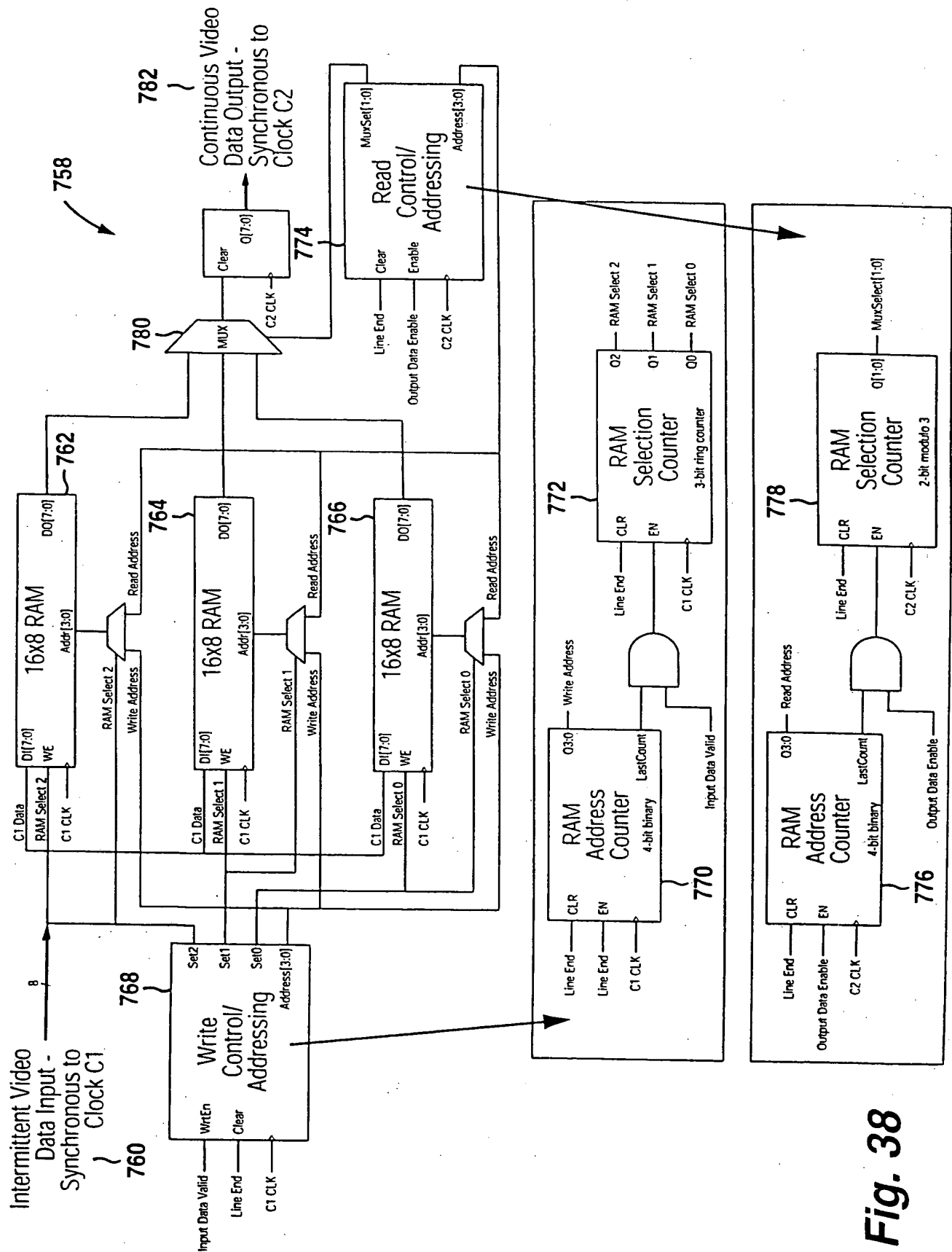


Fig. 38